MP6411

Windowed Watchdog Timer

The Future of Analog IC Technology

DESCRIPTION

The MP6411 is a windowed watchdog timer. It is used to reset and monitor the microcontroller. In normal operation, the MCU sends a trigger signal to the MP6411 in a defined time window cyclically. A missing or fault trigger signal causes the watchdog to reset the MCU.

The MP6411 provides a reset signal (low-level voltage) to the MCU during power-up or under voltage.

By setting MODE to high or low, the watchdog operates in long window mode or short window mode; the window is programmable.

The MP6411 is available in SOIC8 package.

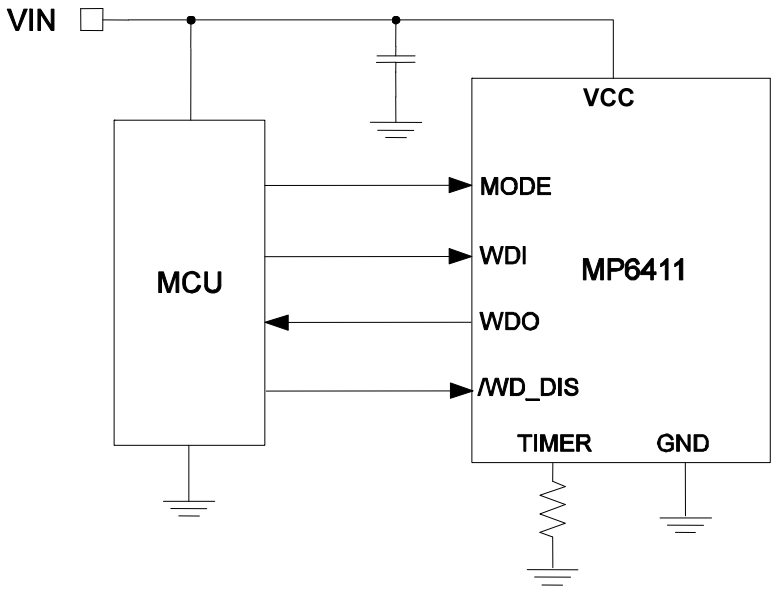
FEATURES

- Windowed Watchdog
- Power-On Reset during Power-Up and Under Voltage
- Programmable Short Window Mode or Long Window Mode
- Watchdog Disable Function
- Low Shutdown Mode Current
- SOIC8 Package

APPLICATIONS

- Automotive Systems
- Industrial Systems

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6411GS	SOIC-8	*See Below*

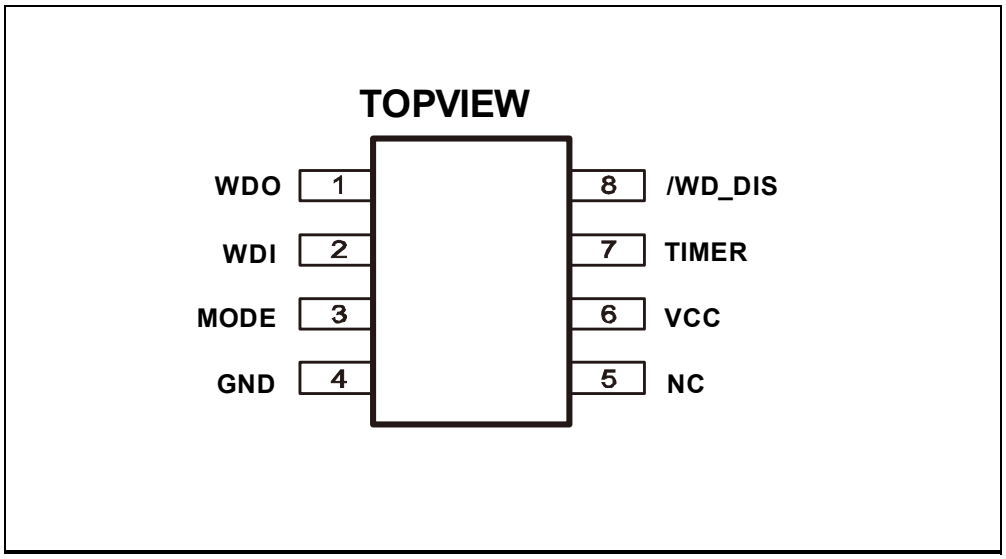
* For Tape & Reel, add suffix –Z (e.g. MP6411GS–Z);

TOP MARKING

MP6411
LLLLLLLL
MPSYWW

MP6411: Product code of MP6411GS
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

All pins ……..-0.3V to +6V
Continuous power dissipation (T_A = +25°C) (2)
SOIC8 …… ..... ……1.3W
Junction temperature…….. ……150°C
Lead temperature …… ..... ……260°C
Storage temperature…….. -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN})……..... 5V
Operating junction temp. (T_J)..... -40°C to 125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC-8…..……96……45…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Timer voltage		R_{TIMER} = 51k		0.3		V
Quiescent current	I_Q	R_{TIMER} = 100k		16	19	µA
		R_{TIMER} = 51k		25	32	µA
Power on reset threshold	$V_{POR-HIGH}$	WDO goes high with rising V_{CC}	4.4	4.6	4.8	V
	$V_{POR-LOW}$	WDO goes low with falling V_{CC}	4.3	4.5	4.7	V
Timing						
Single period	T	R_{TIMER} = 51k	-10%	880	+10%	µs
Power on delay(5)	t_0	R_{TIMER} = 51k		10		cycle
Sync signal monitoring time(5)	t_1	R_{TIMER} = 51k		450		cycle
Watchdog window close time (short mode)(5)	t_2	R_{TIMER} = 51k, mode = low		15		cycle
Watchdog window open time (short mode) (5)	t_3	R_{TIMER} = 51k, mode = low		10		cycle
Watchdog window close time (long mode) (5)	t_4	R_{TIMER} = 51k, mode = high		1500		cycle
Watchdog window open time (long mode) (5)	t_5	R_{TIMER} = 51k, mode = high		1000		cycle
WDO reset pulse width(5)	t_6	R_{TIMER} = 51k		4		cycle
WDI_OK pulse width			10		5000	µs
Input and Output						
WDI logic high			3.2			V
WDI logic low					0.8	V
MODE logic high			3.2			V
MODE logic low					0.8	V
MODE input Current		MODE = 5V		0.1	1	µA
		MODE = 0V		5	8	µA
/WD_DIS logic high			3.2			V
/WD_DIS logic low					0.8	V
/WD_DIS input Current		WD_DIS = 5V		0.1	1	µA
		WD_DIS = 0V		5	8	µA
WDO high		VCC = 5V, I_{WDO} = 1mA	V_{CC}-0.2			V
WDO low		VCC = 5V, I_{WDO} = 1mA			0.2	V
		VCC = 1V, I_{WDO} = 300µA			0.1	V

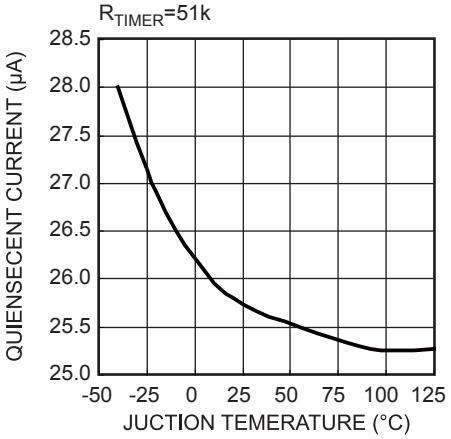
Notes:

5) Derived from bench characterization. Not tested in production.

TYPICAL CHARATERISTICS

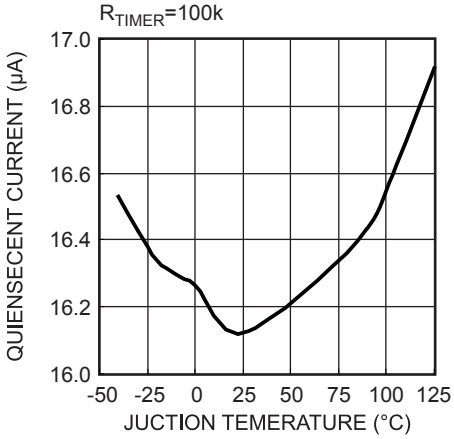
Quiescent Current vs. Junction Temerature

R_{TIMER}=51k



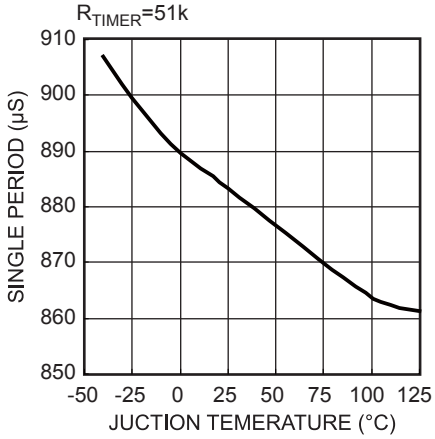
Quiescent Current vs. Junction Temerature

R_{TIMER}=100k



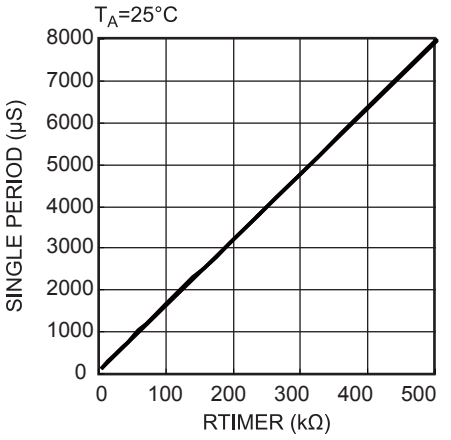
Single Period vs. Junction Temerature

R_{TIMER}=51k



Single Period vs. RTIMER

T_A=25°C



PIN FUNCTION

Pin #	Name	Description
1	WDO	Watchdog output. WDO outputs a reset signal to the MCU.
2	WDI	Watchdog input. WDI receives the trigger signal from the MCU.
3	MODE	Mode switching pin. Pull MODE high to make the watchdog operate in long window mode; pull MODE low to make it work in short window mode. MODE has a weak internal pull-up.
4	GND	Ground.
5	NC	Not connected.
6	VCC	Power input. A 0.1μF ceramic capacitor is recommended to put between VCC and GND pins.
7	TIMER	Watchdog timer pin. TIMER sets the time-out with an external resistor
8	/WD_DIS	Watchdog disable pin. Pull /WD_DIS low to disable the watchdog; pull /WD_DIS high to enable the watchdog. It has a weak internal pull-up.

FUNCTIONAL BLOCK DIAGRAM

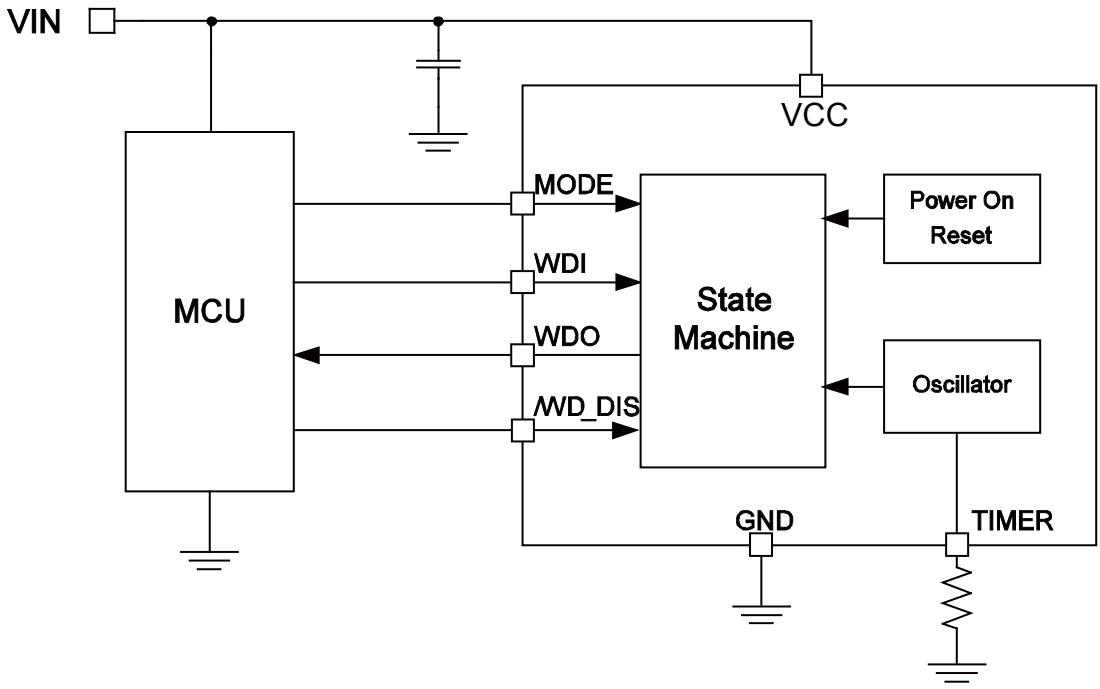
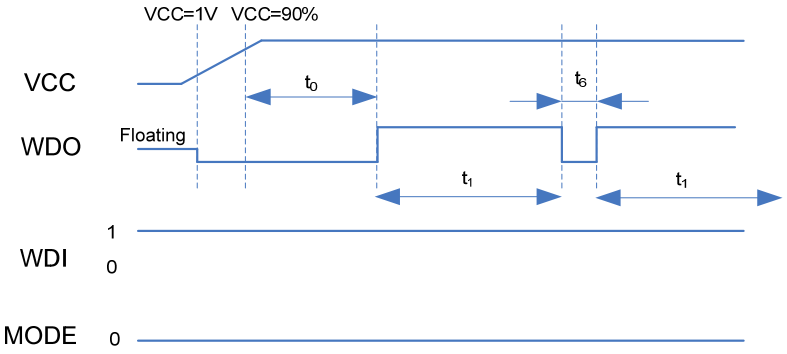


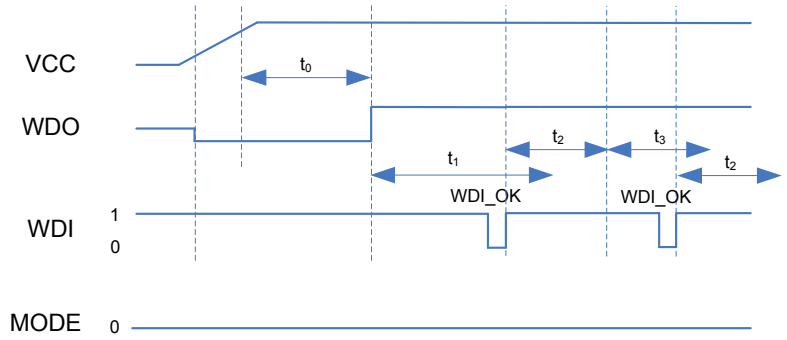
Figure 1: Functional Block Diagram

TIMING DIAGRAM

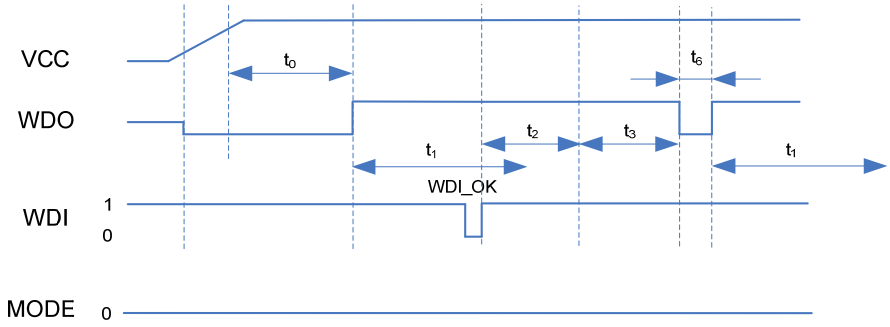
Power-on reset and no sync signal



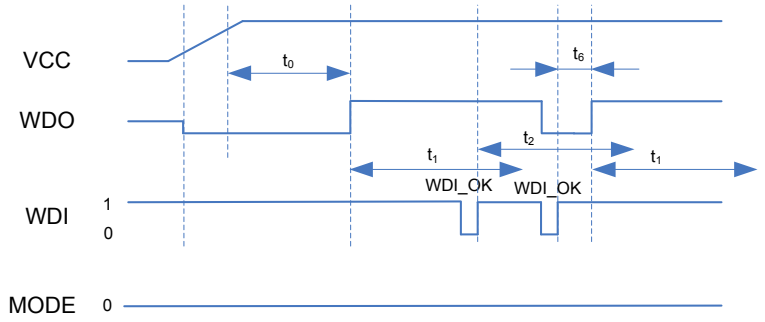
Synchronized by WDI and triggered in open window (MODE=0, short window mode)



Synchronized by WDI and no trigger signal (MODE=0, short window mode)

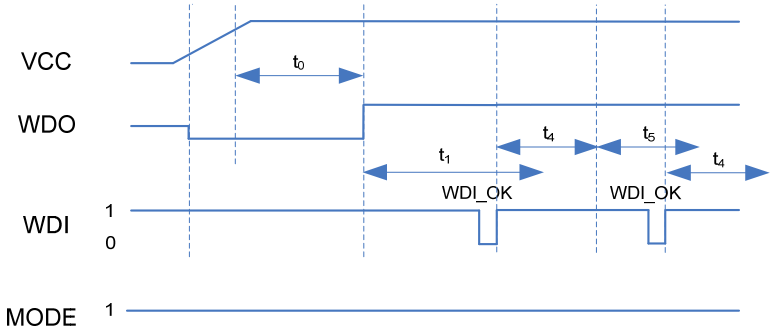


Synchronized by WDI and triggered in closed window (MODE=0, short window mode)

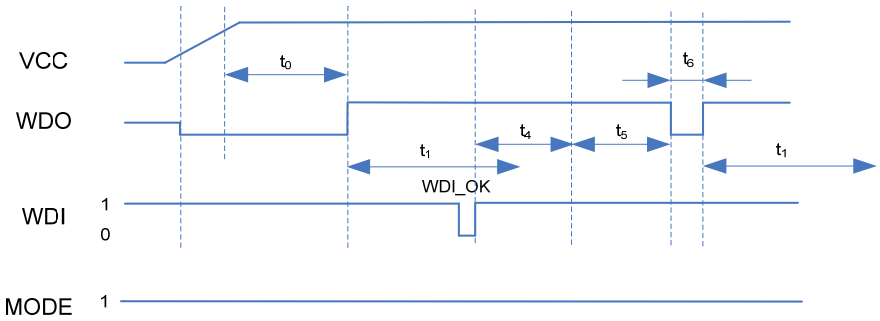


Note: When the WDI_OK rising edge that comes at WDO is low, the t_6 timer will be reset. Therefore, in the situation above, the WDO reset signal maintains a t_6+WDI_OK time.

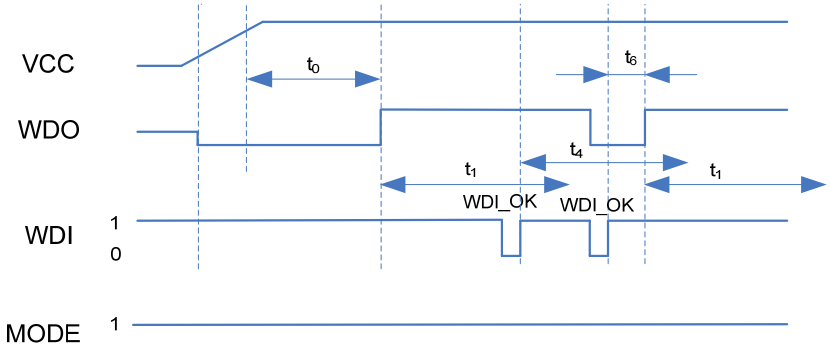
Synchronized by WDI and triggered in open window (MODE=1, long window mode)



Synchronized by WDI and no trigger signal (MODE=1, long window mode)

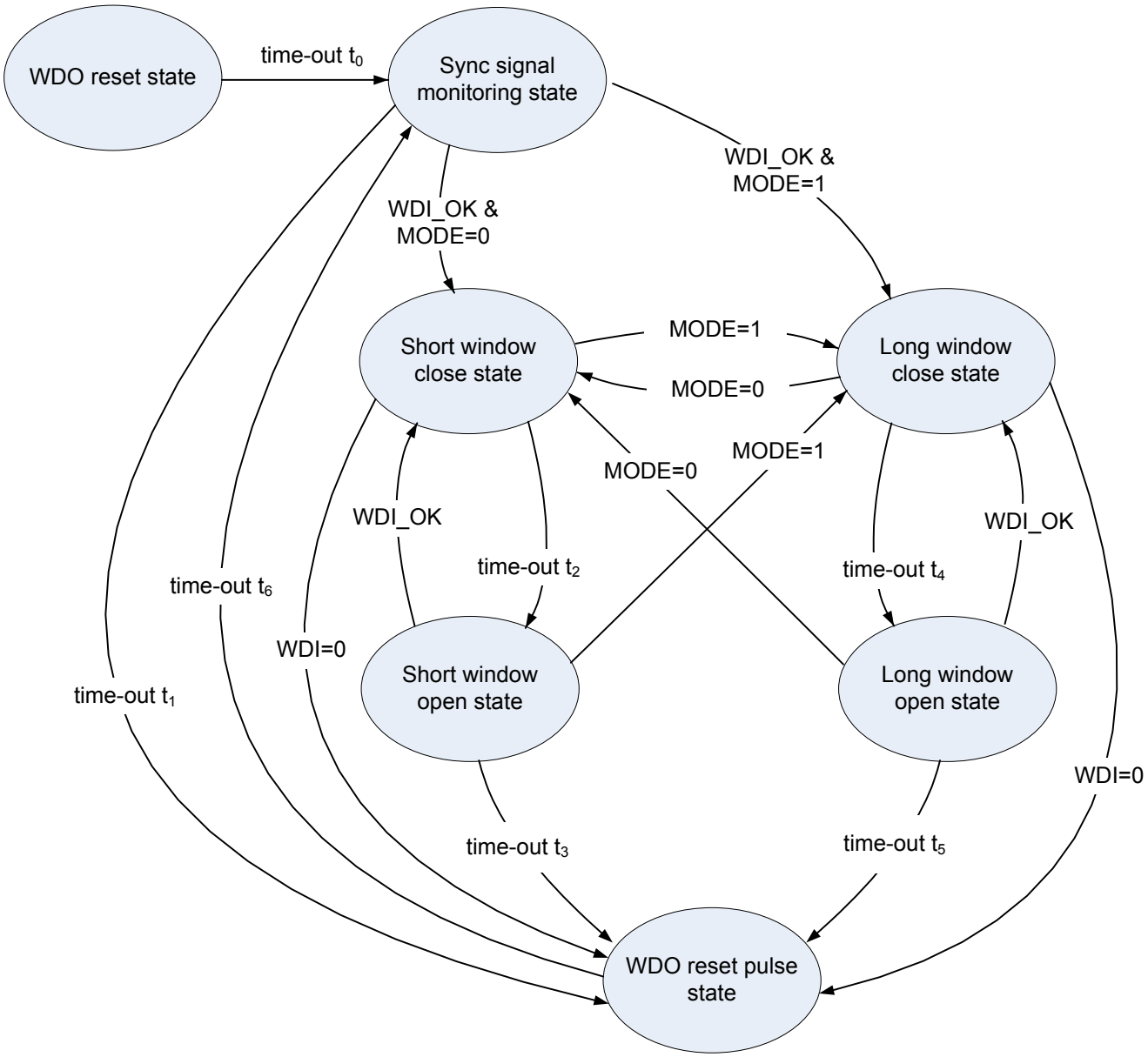


Synchronized by WDI and triggered in closed window (MODE=1, long window mode)



Note: When the WDI_OK rising edge that comes at WDO is low, the t_6 timer will be reset. Therefore, in the situation above, the WDO reset signal maintains a t_6+WDI_OK time.

STATE DIAGRAM



Note: The state diagram above does not include if a WDI error occurs.

OPERATION

Supply Voltage

V_{CC} = 5V +/-10% is recommended for normal operation. WDO is pulled low when Vcc rises to 1V or above. After Vcc rises to 4.65V (typically), WDO will remain at a low level for t_0 to reset the MCU.

TIMER

Period T (μs):

$$T(\mu s) = 15.75 \times R_{TIMER}(k\Omega) + 73.5$$

R_{TIMER} (kΩ):

$$R_{TIMER}(k\Omega) = 0.063 \times T(\mu s) - 4.67$$

For example: R_{TIMER}=51kΩ, T≈0.88ms

Monitor MCU Synchronization Signal

When the watchdog is in a "sync signal monitoring state," the following will occur:

- If the watchdog IC receives a WDI_OK signal from the MCU within t_1 (WDI remains low for 10μs to 5ms), the timer will be reset, and the watchdog works in normal operation.
- If the watchdog does not receive the WDI_OK signal from the MCU during t_1, it will generate a reset signal and go into "sync signal monitor state" again.

Short Window Mode

If the MCU and watchdog are synchronized correctly and MODE is low, the watchdog will work in short window mode:

- If WDI_OK is received in a window close state (t_2), the watchdog outputs a reset signal and goes into a sync signal monitoring state.
- If WDI_OK is received in a window open state (t_3), the watchdog goes into a window close state. The MCU works in normal operation in this situation.
- If no WDI_OK signal is received in t_2+t_3, the watchdog outputs a reset signal and goes into a sync signal monitoring state.
- If MODE is pulled high during short window mode, the watchdog will go into long window mode.

Long Window Mode

If the MCU and watchdog are synchronized correctly and MODE is high, the watchdog will operate in long window mode, and the following will occur:

- If WDI_OK is received in a window close state (t_4), the watchdog outputs a reset signal and goes into a sync signal monitoring state.
- If WDI_OK is received in a window open state (t_5), the watchdog goes into a window close state. The MCU works in normal operation in this situation.
- If no WDI_OK signal is received in t_4+t_5, the watchdog outputs a reset signal and goes into a sync signal monitoring state.
- If MODE is pulled low during a long window mode, the watchdog will go into a short window mode.

Watchdog Disable

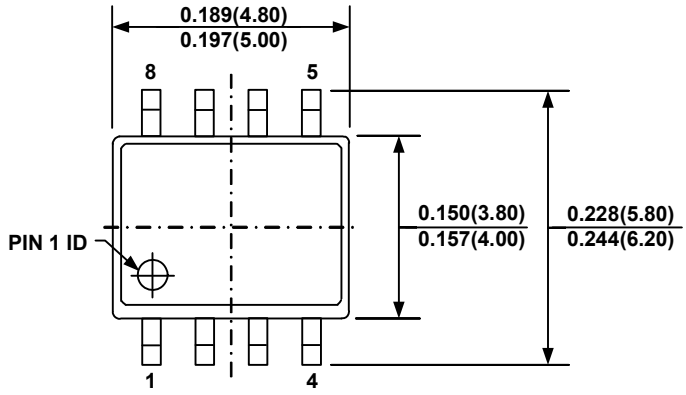
Pull /WD_DIS low to disable the watchdog; pull it high to enable the watchdog. /WD_DIS has a weak internal pull-up, so the watchdog is enabled if /WD_DIS is left open.

WDI Error

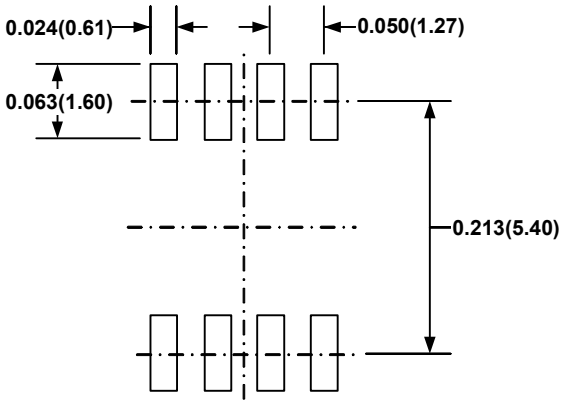
If a WDI signal remains at a low level for longer than the maximum WDI_OK pulse width, it is regarded as an error. When this error occurs, WDO is pulled down until WDI returns to a high level.

PACKAGE INFORMATION

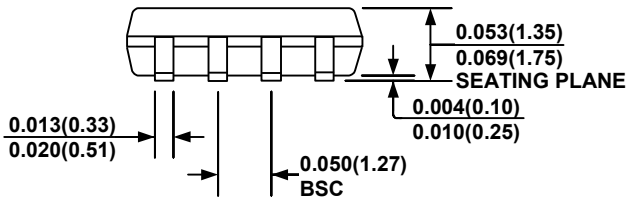
SOIC-8



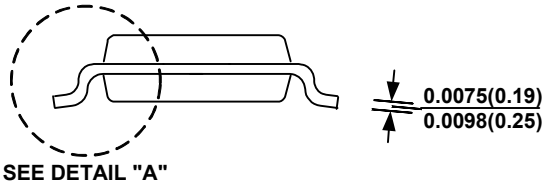
TOP VIEW



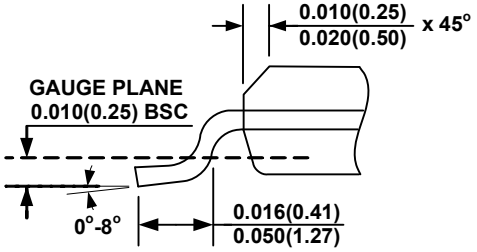
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.