SRR Series, Radial, C³ Technology, X7R Dielectric, 50 – 200 VDC (Commercial Grade)

Overview

KEMET's SRR Series radial through-hole ceramic capacitors in X7R dielectric feature proprietary Ceramic Cased Capacitor (C³) Technology and are designed to meet the needs of critical, high reliability and higher temperature applications. C³ Technology features a unique lead attach configuration with direct internal connection to the Multilayer Ceramic Capacitor (MLCC) electrode system. This configuration promotes superior "pull away" performance and uniform coefficient of linear expansion characteristics at elevated temperatures when compared to conventional through-hole technologies. Design details are outlined in U.S Patent Number 4931899.

X7R dielectric features a 125°C maximum operating temperature and is considered "temperature stable." The Electronics Industries Alliance (EIA) characterizes X7R dielectric as a Class II material. Components of this classification are fixed, ceramic dielectric capacitors suited for bypass and decoupling applications or for frequency discriminating circuits where Q and stability of capacitance characteristics are not critical. X7R exhibits a predictable change in capacitance with respect to time and voltage and boasts a minimal change in capacitance with reference to ambient temperature. Capacitance change is limited to ±15% from −55°C to +125°C.

Benefits

- Radial through-hole form factor
- Non-encapsulated
- Proprietary and robust C³ Technology design
- 0.200" and 0.400" lead spacing
- −55°C to +125°C operating temperature range
- DC voltage ratings of 50 V, 100 V and 200 V
- Capacitance offerings ranging from 680 pF up to 4.7 µF
- Available capacitance tolerances of ±5%, ±10% and ±20%
- Temperature stable dielectric
- Non-polar device, minimizing installation concerns
- SnPb-coated lead finish (60/40)
- Gold-plated lead finish option available upon request (RoHS)

Ordering Information

S	R	R	09	D	475	J	W	S	
Specification/ Series	Dielectric	Lead Configuration	Style/Size	Rated Voltage (VDC)	Capacitance Code (pF)	Capacitance Tolerance[1]	Lead Finish[2]	Screening Option	Packaging/ Grade (C-Spec)
S=Standard	R = X7R	R =Radial	05 06 07 08 09	B = 50 V D = 100 V F = 200 V	Two significant digits and number of zeros	J = ±5% K = ±10% M = ±20%	W = SnPb (60/40) G = Au	S = Standard A = Group A (MIL–PRF–39014)	Blank = Tray

[1] *Additional capacitance tolerance offerings may be available. Contact KEMET for details.*
[2] *Lead materials:*
Standard: 60% tin (Sn)/40% lead (Pb) finish with 100% copper core ("C" designation).
Alternative lead materials and finishes may be available. Contact KEMET for details.

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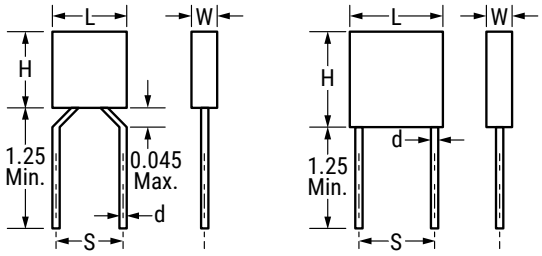
Dimensions – Inches (Millimeters)



Series	Style/ Size	S Lead Spacing	L Length Maximum	H Height Maximum	T Thickness Maximum	LD Lead Diameter	LL Lead Length Minimum
SRR	05	0.20±0.015 (5.08±0.38)	0.200 (5.08)	0.200 (5.08)	0.100 (2.54)	0.020±0.002 (0.508±0.051)	1.25 (31.75)
	06		0.300 (7.62)	0.300 (7.62)	0.100 (2.54)		
	07		0.300 (7.62)	0.300 (7.62)	0.150 (3.81)		
	08	0.40±0.02 (10.16±0.51)	0.500 (12.70)	0.500 (12.70)	0.100 (2.54)	0.025±0.002 (0.635±0.051)	
	09		0.500 (12.70)	0.500 (12.70)	0.150 (3.81)		

Applications

Typical applications include decoupling, bypass, line filtering, transient voltage suppression and frequency discrimination.

Qualification/Certification

Commercial Grade products are subject to internal qualification. Details regarding test methods and conditions are referenced in Table 2, Performance & Reliability.

Environmental Compliance

Devices with standard lead finish option of 60% tin (Sn)/40% lead (Pb) do not meet RoHS criteria.
Devices with gold (AU) lead finish option are RoHS compliant.

Electrical Parameters/Characteristics

Item	Parameters/Characteristics
Operating Temperature Range	−55°C to +125°C
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	±15%
Aging Rate (Maximum % Cap Loss/Decade Hour)	3.0%
Dielectric Withstanding Voltage	250% of rated voltage (5±1 second and charge/discharge not exceeding 50 mA)
Dissipation Factor (DF) Maximum Limit at 25ºC	3.5%(25 V) and 2.5%(50 V to 200 V)
Insulation Resistance (IR) Limit at 25°C	1,000 megohm microfarads or 100 GΩ (Rated voltage applied for 120±5 seconds at 25°C)

Regarding aging rate: Capacitance measurements (including tolerance) are indexed to a referee time of 1,000 hours.
To obtain IR limit, divide MΩ-µF value by the capacitance and compare to GΩ limit. Select the lower of the two limits.
Capacitance and dissipation factor (DF) measured under the following conditions:

1 MHz ±100 kHz and 1.0 V_{rms} ±0.2 V if capacitance ≤ 1,000 pF

1 kHz ±50 Hz and 1.0 V_{rms} ±0.2 V if capacitance > 1,000 pF

Note: When measuring capacitance it is important to ensure the set voltage level is held constant. The HP4284 and Agilent E4980 have a feature known as Automatic Level Control (ALC). The ALC feature should be switched to "ON."

Post Environmental Limits

High Temperature Life, Biased Humidity, Moisture Resistance				
Dielectric	Rated DC Voltage	Capacitance Value	DF (%)	Capacitance Shift
X7R	> 25	All	3.0	±20%
	16/25		5.0	
	< 16		7.5	

Table 1A – SRR05 Style/Size (0.200" Lead Spacing), Capacitance Range Waterfall

SRR05 Style/Size (0.200" Lead Spacing)				
Rated Voltage (VDC)		**50**	**100**	**200**
Voltage Code		**B**	**D**	**F**
Capacitance	**Capacitance Tolerance**	**Capacitance Code (Available Capacitance)**		
680pF	J = ±5% K = ±10% M = ±20%	681	681	
820pF		821	821	
1000pF		102	102	102
1200pF		122	122	122
1500pF		152	152	152
1800pF		182	182	182
2200pF		222	222	222
2700pF		272	272	272
3300pF		332	332	332
3900pF		392	392	392
4700pF		472	472	472
5600pF		562	562	562
6800pF		682	682	682
8200pF		822	822	822
0.01µF		103	103	103
0.012µF		123	123	123
0.015µF		153	153	153
0.018µF		183	183	183
0.022µF		223	223	223
0.027µF		273	273	273
0.033µF		333	333	333
0.039µF		393	393	393
0.047µF		473	473	473
0.056µF		563	563	563
0.068µF		683	683	683
0.1µF		104	104	104
0.12µF		124	124	
0.15µF		154	154	
0.18µF		184	184	
0.22µF		224	224	
0.27µF		274	274	
0.33µF		334	334	
Rated Voltage (VDC)		**50**	**100**	**200**
Voltage Code		**B**	**D**	**F**

Table 1B – SRR06 Style/Size (0.200" Lead Spacing), Capacitance Range Waterfall

SRR06 Style/Size (0.200" Lead Spacing)				
Rated Voltage (VDC)		**50**	**100**	**200**
Voltage Code		**B**	**D**	**F**
Capacitance	**Capacitance Tolerance**	**Capacitance Code (Available Capacitance)**		
0.01µF	J = ±5% K = ±10% M = ±20%	103	103	103
0.012µF		123	123	123
0.015µF		153	153	153
0.018µF		183	183	183
0.022µF		223	223	223
0.027µF		273	273	273
0.033µF		333	333	333
0.039µF		393	393	393
0.047µF		473	473	473
0.056µF		563	563	563
0.068µF		683	683	683
0.1µF		104	104	104
0.12µF		124	124	124
0.15µF		154	154	154
0.18µF		184	184	184
0.22µF		224	224	224
0.27µF		274	274	274
0.33µF		334	334	334
0.39µF		394	394	394
0.47µF		474	474	
0.56µF		564	564	
0.68µF		684	684	
0.82µF		824	824	
1.0µF		105	105	
Rated Voltage (VDC)		**50**	**100**	**200**
Voltage Code		**B**	**D**	**F**

Table 1A – SRR07 Style/Size (0.200" Lead Spacing), Capacitance Range Waterfall

SRR07 Style/Size (0.200" Lead Spacing)				
Rated Voltage (VDC)		**50**	**100**	**200**
Voltage Code		**B**	**D**	**F**
Capacitance	**Capacitance Tolerance**	**Capacitance Code (Available Capacitance)**		
0.01µF	J = ±5% K = ±10% M = ±20%	103	103	103
0.012µF		123	123	123
0.015µF		153	153	153
0.018µF		183	183	183
0.022µF		223	223	223
0.027µF		273	273	273
0.033µF		333	333	333
0.039µF		393	393	393
0.047µF		473	473	473
0.056µF		563	563	563
0.068µF		683	683	683
0.1µF		104	104	104
0.12µF		124	124	124
0.15µF		154	154	154
0.18µF		184	184	184
0.22µF		224	224	224
0.27µF		274	274	274
0.33µF		334	334	334
0.39µF		394	394	394
0.47µF		474	474	474
0.56µF		564	564	564
0.68µF		684	684	684
0.82µF		824	824	824
1.0µF		105	105	
1.2µF		125	125	
1.5µF		155	155	
1.8µF		185	185	
Rated Voltage (VDC)		**50**	**100**	**200**
Voltage Code		**B**	**D**	**F**

Table 1D – SRR08 Style/Size (0.400" Lead Spacing), Capacitance Range Waterfall

SRR08 Style/Size (0.400" Lead Spacing)				
Rated Voltage (VDC)		**50**	**100**	**200**
Voltage Code		**B**	**D**	**F**
Capacitance	**Capacitance Tolerance**	**Capacitance Code (Available Capacitance)**		
0.01µF	J = ±5% K = ±10% M = ±20%	103	103	103
0.012µF		123	123	123
0.015µF		153	153	153
0.018µF		183	183	183
0.022µF		223	223	223
0.027µF		273	273	273
0.033µF		333	333	333
0.039µF		393	393	393
0.047µF		473	473	473
0.056µF		563	563	563
0.068µF		683	683	683
0.1µF		104	104	104
0.12µF		124	124	124
0.15µF		154	154	154
0.18µF		184	184	184
0.22µF		224	224	224
0.27µF		274	274	274
0.33µF		334	334	334
0.39µF		394	394	394
0.47µF		474	474	474
0.56µF		564	564	564
0.68µF		684	684	684
0.82µF		824	824	824
1.0µF		105	105	
1.2µF		125	125	
1.5µF		155	155	
1.8µF		185	185	
2.2µF		225	225	
2.7µF		275	275	
Rated Voltage (VDC)		**50**	**100**	**200**
Voltage Code		**B**	**D**	**F**

Table 1E – SRR09 Style/Size (0.400" Lead Spacing), Capacitance Range Waterfall

SRR09 Style/Size (0.400" Lead Spacing)				
Rated Voltage (VDC)		**50**	**100**	**200**
Voltage Code		**B**	**D**	**F**
Capacitance	**Capacitance Tolerance**	**Capacitance Code (Available Capacitance)**		
0.033µF	J = ±5% K = ±10% M = ±20%	333	333	333
0.039µF		393	393	393
0.047µF		473	473	473
0.056µF		563	563	563
0.068µF		683	683	683
0.1µF		104	104	104
0.12µF		124	124	124
0.15µF		154	154	154
0.18µF		184	184	184
0.22µF		224	224	224
0.27µF		274	274	274
0.33µF		334	334	334
0.39µF		394	394	394
0.47µF		474	474	474
0.56µF		564	564	564
0.68µF		684	684	684
0.82µF		824	824	824
1.0µF		105	105	105
1.2µF		125	125	125
1.5µF		155	155	155
1.8µF		185	185	185
2.2µF		225	225	225
2.7µF		275	275	
3.3µF		335	335	
3.9µF		395	395	
4.7µF		475	475	
Rated Voltage (VDC)		**50**	**100**	**200**
Voltage Code		**B**	**D**	**F**

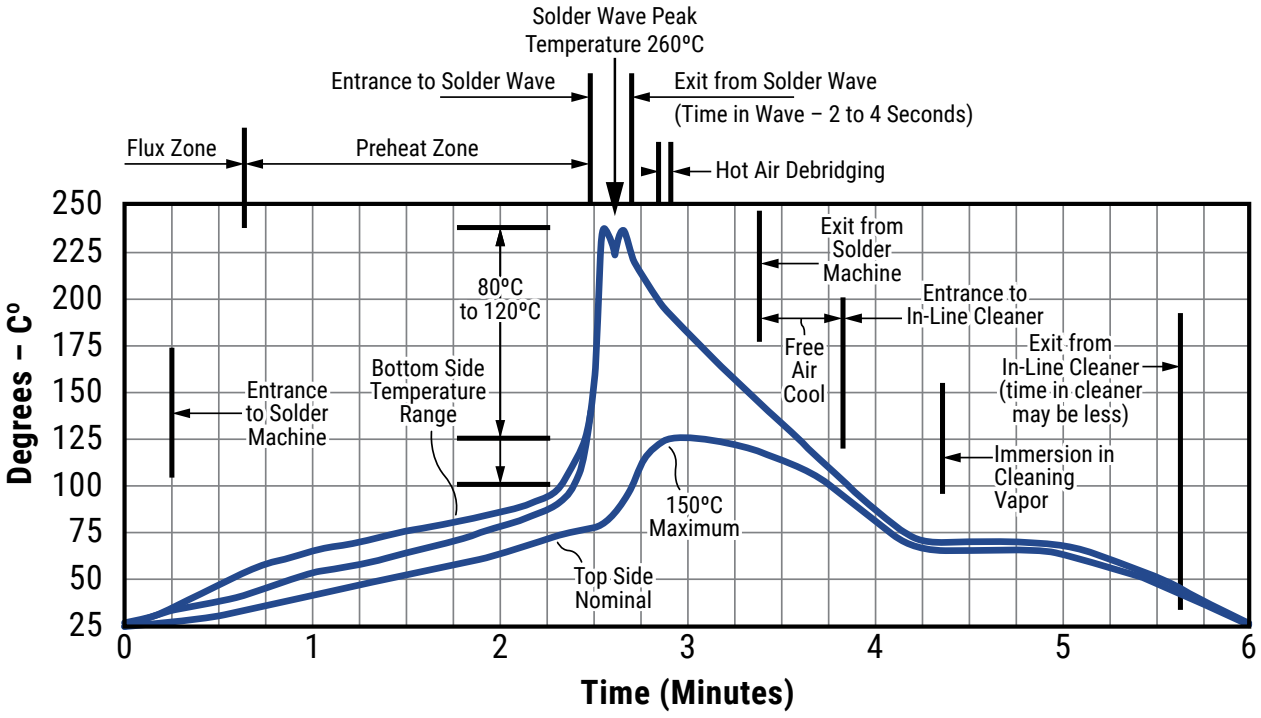
Soldering Process

Recommended Soldering Technique:

- Solder Wave
- Hand Soldering (Manual)

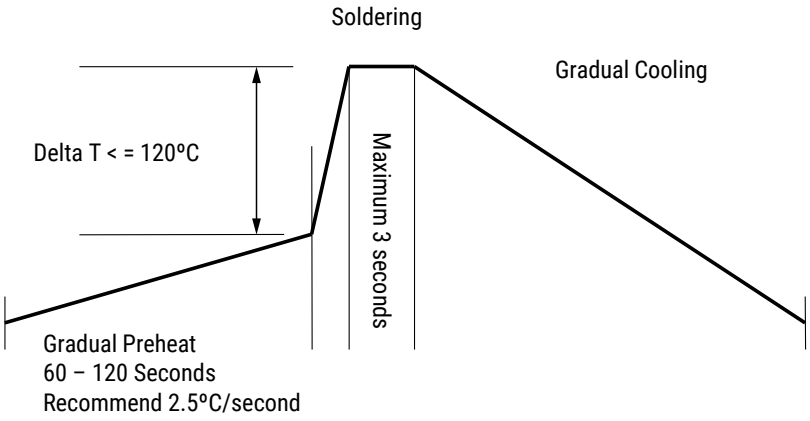
Recommended Soldering Profile:

- Optimum Wave Solder Profile



- Hand Soldering (Manual)

Manual Solder Profile with Pre-heating



KEMET recommends following the guidelines and techniques outlined in technical bulletins F2103 and F9207.

Table 2 – Performance & Reliability: Test Methods and Conditions

Stress	Reference	Test or Inspection Method
Solderability	J–STD–002	Magnification 50 X. Conditions:
		a) Method B, 4 hours at 155°C, dry heat at 235°C
		b) Method B at 215°C category 3
		c) Method D, category 3 at 260°C
Temperature Cycling	JESD22 Method JA–104	1,000 cycles (–55°C to +125°C), Measurement at 24 hours. +/–2 hours after test conclusion.
Biased Humidity	MIL–STD–202 Method 103	Load Humidity: 1,000 hours 85°C/85% RH and Rated Voltage. Add 100 K ohm resistor. Measurement at 24 hours. +/–2 hours after test conclusion.
		Low Volt Humidity: 1,000 hours 85°C/85% RH and 1.5 V. Add 100 K ohm resistor. Measurement at 24 hours. +/–2 hours after test conclusion.
Moisture Resistance	MIL–STD–202 Method 106	t = 24 hours/cycle. Steps 7a and 7b not required. Unpowered. Measurement at 24 hours. +/–2 hours after test conclusion.
Thermal Shock	MIL–STD–202 Method 107	–55°C/+125°C. Note: Number of cycles required – 300. Maximum transfer time – 20 seconds. Dwell time – 15 minutes. Air – Air.
High Temperature Life	MIL–STD–202 Method 108 /EIA–198	1,000 hours at 125°C (85°C for X5R, Z5U and Y5V) with 2 X rated voltage applied.
Storage Life	MIL–STD–202 Method 108	150°C, 0 VDC, for 1,000 hours.
Vibration	MIL–STD–202 Method 204	5 g for 20 minutes, 12 cycles each of 3 orientations. Note: Use 8"X5" PCB .031" thick 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10 – 2,000 Hz.
Resistance to Soldering Heat	MIL–STD–202 Method 210	Condition B. No pre-heat of samples. Note: single wave solder – procedure 2.
Terminal Strength	MIL–STD–202 Method 211	Conditions A (2.3 kg or 5 lbs)
Mechanical Shock	MIL–STD–202 Method 213	Figure 1 of Method 213, Condition F.
Resistance to Solvents	MIL–STD–202 Method 215	Add aqueous wash chemical, OKEM Clean or equivalent.

Storage & Handling

Ceramic chip capacitors should be stored in normal working environments. While the chips themselves are quite robust in other environments, solderability will be degraded by exposure to high temperatures, high humidity, corrosive atmospheres, and long term storage. In addition, packaging materials will be degraded by high temperature–reels may soften or warp, and tape peel force may increase. KEMET recommends that maximum storage temperature not exceed 40ºC, and maximum storage humidity not exceed 70% relative humidity. Temperature fluctuations should be minimized to avoid condensation on the parts, and atmospheres should be free of chlorine and sulfur bearing compounds. For optimized solderability, chip stock should be used promptly, preferably within 1.5 years of receipt.

Packaging Details

Lead Spacing	Component Pitch (P1)
0.100 (2.54)	5.08
0.200 (5.08)	3.81
0.400 (10.16)	7.62
0.170 (4.32)	
0.220 (5.59)	
0.275 (6.98)	
0.300 (7.62)	
0.375 (9.52)	
0.475 (12.06)	
0.575 (14.60)	
0.675 (17.14)	

Packaging Quantities

Series	Style/Size	Tray Quantity Minimum[1]	Tray Quantity Maximum[1]
SCR	05	1	56
	06		28
	07		
	08		20
	09		

[1] *Minimum order value applies. Contact KEMET for details.*

Marking

Manufacturer's ID	KEC
Capacitance	106J
Voltage	50V
Date Code	123

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