

Audio Jack Detector and Pop Noise Control Switch

DESCRIPTION

The DG2591 is an audio jack detector and pop noise control switch IC.

When there is no ear phone detected, the DG2591 connects the microphone bias line to ground through the MIC pin. The DG2591 also gives a logic HIGH signal to the baseband controller through the OUT pin.

The DG2591 senses the DC levels at both L_Detect and GND_Detect. When an ear phone is plugged in, the voltage at both pins will go low. The DG2591 will indicate the presence of the ear phone by pulling OUT low and the MIC switch will turn off.

The DG2591 is available ultra small miniQFN6 of 1 mm x 1.2 mm size.

FEATURES

- Operates with 1.8 V ± 5 %
- Low quiescent current of 2 μA/max.
- Integrated sense comparator for audio L of 1.4 V ± 5 % threshold
- 1 Ω/max. MIC bias switch provides a quick discharge and clamping
- (Integrated deglitch circuit)
- ESD Protected
 - Human body model > 5 kV
 - Charged device model > 1 kV
 - IEC 61000-4-2 air discharge > 15 kV
 - IEC 61000-4-2 contact discharge > 8 kV
- Ultra compact miniQFN6 of 1 mm x 1.2 mm
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Cellular phones
- Tablet devices
- Portable media players
- · Digital cameras

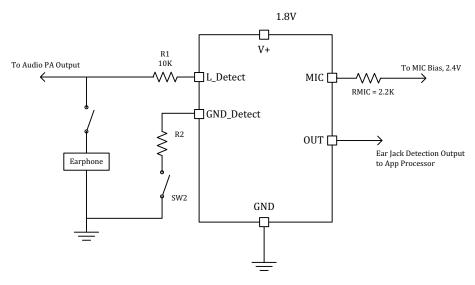


Fig. 1 - Typical Operation Circuit





PACKAGE OUTLINE

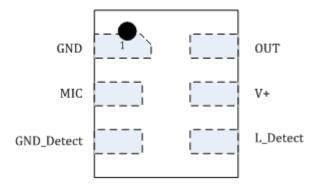
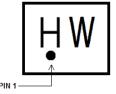


Fig. 2 - Device Pin Out miniQFN6 Top View, Pin 1 Dot Marking is on Top of the Device

PIN DESCRIPTION					
PIN#	NAME	FUNCTION			
1	GND	Ground			
2	MIC	Microphone bias switch input. Connect to AUXMIC_IN			
3	GND_Detect	Connect to ground detect pin at audio jack			
4	L_Detect	Connected to L_Detect pin at audio jack			
5	V+	Device power supply connected to 1.8 V source			
6	OUT	Detect logic output connected to baseband controller			

ORDERING INFORMATION						
TEMPERATURE RANGE	PACKAGE	PART NUMBER				
-40 °C to 85 °C	miniQFN6	DG2591DN-T1-GE4				

DEVICE MARKING



H = DG2591 Marking Code, W = Date/Lot Traceability Code



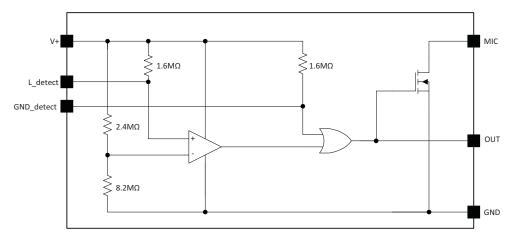


Fig. 3 - Functional Block Diagram

TRUTH TABLE							
L_DETECT	GND_DETECT	OUT	MIC				
0	0	Low	High				
1	х	High	Low				
х	1	High	Low				

ABSOLUTE MAXIMUM RA	TINGS				
PINS OR PARAMETERS	CONDITIONS	LIMITS	UNIT		
V+	Reference to GND		-0.3 to 6		
L_Detect, GND_Detect, OUT	Reference to GND		V+	V	
MIC			-0.3 to 6	1	
Storage Temperature			-65 to +150	°C	
MSL	Moisture Sensitivity Level (JEDEC® J-STD-	Moisture Sensitivity Level (JEDEC® J-STD-020)			
I _{MIC}	Switch DC current	200			
Імісреак	Switch peak current (pulsed at 1 ms, < 10	500	mA		
Latch up Current per JESD78			500		
	Human body model	> 5			
ESD	IEC 61000-2-4, Level 4, L_Detect,	Contact	> 8	kV	
E9D	GND_Detect, MIC and GND Pins	Air	> 15	KV	
	Charged device model, JESD22-C101	>1			
RECOMMENDED OPERATING CON	DITION				
V+			1.8	V	
Operating Junction Temperature		-40 ~ +125	°C		

Notes

- The control logic pins should not float. It should be compliant with either high or low logic
- Negative current injection up to 300 mA

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

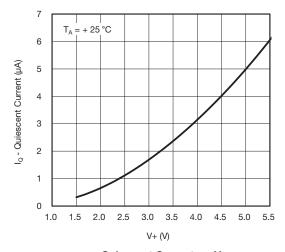


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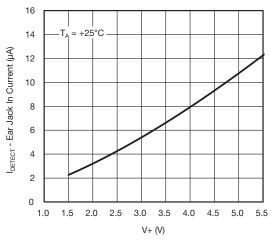
Type			TEST CONDITION	LIMITS				
Ear Jack In Current Detect V+ = 1.8 V; L_Detect, GND_Detect are connected with 10 kΩ to GND V+ = 1.8 V; L_Detect Are connected with 10 kΩ to GND V+ = 1.8 V V V V V V V V V V	PARAMETER	SYMBOL	$T_A = -40 ^{\circ}\text{C} \text{ to } 85 ^{\circ}\text{C},$	MIN.	TYP.	MAX.	UNIT	
L_Detect Reference Vittl 10 kΩ to GND_Detect Vittl	Quiescent Current	IQ	V+ = 1.8 V; L_Detect, GND_Detect are open	-	< 1	2		
Voltage Vol	Ear Jack In Current	I _{DETECT}		-	-	5	μΑ	
Voltage Hysteresis GND_Detect = 0 V	L_Detect Reference Voltage		1.33 1.4 1.47			V		
Logic Low Voltage	L_Detect Reference Voltage Hysteresis		GND_Detect = 0 V	-	20	-	mV	
Continue	GND_Detect Logic Low Voltage		V+ = 1.8 V	0.6	0.84	-	V	
Resistance HMIC L_Detect, GND_Detect = Open - - 1 1 1 1 1 1 1 1	GND_Detect Logic High Voltage		V+ = 1.8 V	-	-	1.1	V	
OUT Pull Up RourH V+ = 1.8 V; L_Detect, GND_Detect = Open 110 Ω	MIC Switch Resistance	R _{MIC}		-	-	1	Ω	
Resistance Houth L_Detect, GND_Detect = Open - -	MIC Leakage		V _{MIC} = 2.4 V	-1	-	1	μA	
Nout	OUT Pull Up Resistance	R _{OUT} H	1	-	-	110		
Voltage VOUTH L_Detect, GND_Detect = Open UT Low Logic Voltage Vout L V+ = 1.8 V; R _{OUT} = 10 kΩ - - - 0.3 MIC Rising Propagation Delay (insertion detection time) t _{MIC} R From SW1 and SW2 ON, GND_Detect = 0 V, voltage on L_Detect drops to 0.9 V, to the time when MIC rises to 1.2 V and OUT falls below 0.3 V (refer to circuit below, R3 = 10K, C1 = 5 pF, MIC biased at 2.4 V via a 2.2K resistor) - 1.5 2 μs MIC Falling From SW1 and SW2 ON, GND_Detect = 0 V, voltage on L_Detect rises to 0.9 V, to the time when MIC drops to 1.2 V and OUT rises above 0.3 V (refer to circuit below, R3 = 10K, C1 = 5 pF, MIC biased at 2.4 V via a 2.2K resistor) - 350 500 ns OUT Falling Propagation Delay toutF From SW1 and SW2 ON, GND_Detect = 0 V, voltage on L_Detect drops to 0.9 V, to the time when MIC rises to 1.2 V and OUT falls below 0.3 V (refer to circuit below, R3 = 10K, C1 = 5 pF, MIC biased at 2.4 V via a 2.2K resistor) - 1.4 2 μs OUT Rising From SW1 and SW2 ON, GND_Detect = 0 V, voltage on L_Detect rises to 0.9 V, to the time when MIC drops to 1.2 V and OUT rises above 0.3 V (refer to circuit below, R3 = 10K, C1 = 5 pF, MIC biased at 2.4 V via a 2.2K resistor) - 350 500 ns	OUT Pull Down Resistance	R _{OUT} L	L_Detect, GND_Detect are connected with 10 k Ω to	-	-	100	Ω	
OUT Low Logic Voltage VouTL L_Detect, GND_Detect are connected with 10 kΩ to GND, From SW1 and SW2 ON, GND_Detect = 0 V, voltage on L_Detect drops to 0.9 V, to the time when MIC rises to 1.2 V and OUT falls below 0.3 V (refer to circuit below, R3 = 10K, C1 = 5 pF, MIC biased at 2.4 V via a 2.2K resistor) MIC Falling Propagation Delay (removal detection time) ThicF TouTF TouTR TouTR TouTR TouTR L_Detect, GND_Detect are connected with 10 kΩ to GND. From SW1 and SW2 ON, GND_Detect = 0 V, voltage on L_Detect rises to 0.9 V, to the time when MIC drops to 1.2 V and OUT rises above 0.3 V (refer to circuit below, R3 = 10K, C1 = 5 pF, MIC biased at 2.4 V via a 2.2K resistor) From SW1 and SW2 ON, GND_Detect = 0 V, voltage on L_Detect drops to 0.9 V, to the time when MIC rises to 1.2 V and OUT falls below 0.3 V (refer to circuit below, R3 = 10K, C1 = 5 pF, MIC biased at 2.4 V via a 2.2K resistor) OUT Rising Propagation Delay OUT Rising Propagation Delay OUT Rising Propagation Delay TouTR	OUT High Logic Voltage	V _{OUT} H		1.6	-	-		
Propagation Delay (insertion detection time) t _{MICR} t	OUT Low Logic Voltage	V _{OUT} L	L_Detect, GND_Detect are connected with 10 kΩ to	-	-	0.3	V	
Propagation Delay (removal detection time) t _{MIC} F t _{MIC} F t _{MIC} F on L_Detect rises to 0.9 V, to the time when MIC drops to 1.2 V and OUT rises above 0.3 V (refer to circuit below, R3 = 10K, C1 = 5 pF, MIC biased at 2.4 V via a 2.2K resistor) From SW1 and SW2 ON, GND_Detect = 0 V, voltage on L_Detect drops to 0.9 V, to the time when MIC rises to 1.2 V and OUT falls below 0.3 V (refer to circuit below, R3 = 10K, C1 = 5 pF, MIC biased at 2.4 V via a 2.2K resistor) OUT Rising Propagation Delay OUT Rising Propagation Delay t _{OUT} R t _{OUT} R t _{OUT} R t _{OUT} R Tout Rising Propagation Delay Tout Rising Rising Propagation Delay Tout Rising Risi	MIC Rising Propagation Delay (insertion detection time)	t _{MIC} R	on L_Detect drops to 0.9 V, to the time when MIC rises to 1.2 V and OUT falls below 0.3 V (refer to circuit below, R3 = 10K, C1 = 5 pF, MIC	-	1.5	2	μs	
OUT Falling Propagation Delay tout	Propagation Delay (removal detection	t _{MIC} F	on L_Detect rises to 0.9 V, to the time when MIC drops to 1.2 V and OUT rises above 0.3 V (refer to circuit below, R3 = 10K, C1 = 5 pF, MIC	-	350	500	ns	
OUT Rising Propagation Delay toutR on L_Detect rises to 0.9 V, to the time when MIC drops to 1.2 V and OUT rises above 0.3 V (refer to circuit below, R3 = 10K, C1 = 5 pF, MIC biased at 2.4 V via a 2.2K resistor) GND_Detect Cap on L_Detect rises to 0.9 V, to the time when MIC drops to 1.2 V and OUT rises above 0.3 V (refer to circuit below, R3 = 10K, C1 = 5 pF, MIC biased at 2.4 V via a 2.2K resistor)	OUT Falling Propagation Delay	t _{оит} F	on L_Detect drops to 0.9 V, to the time when MIC rises to 1.2 V and OUT falls below 0.3 V (refer to circuit below, R3 = 10K, C1 = 5 pF, MIC	-	1.4	2	μs	
	•	t _{оит} R	on L_Detect rises to 0.9 V, to the time when MIC drops to 1.2 V and OUT rises above 0.3 V (refer to circuit below, R3 = 10K, C1 = 5 pF, MIC	-	350	500	ns	
	GND_Detect Capacitance	C _{GD}		-	-	5	pF	



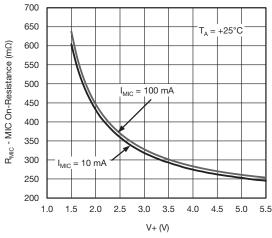
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



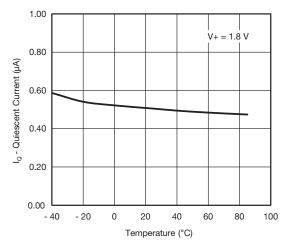
Quiescent Current vs. V+



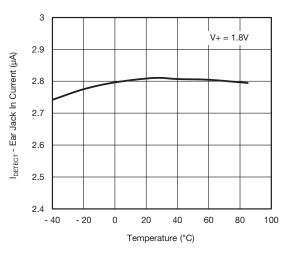
Ear Jack In Current vs. V+



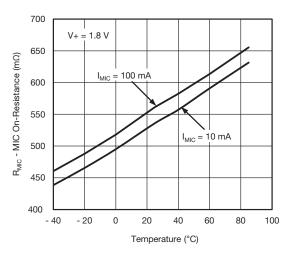
MIC On Resistance vs. V+



Quiescent Current vs. Temperature



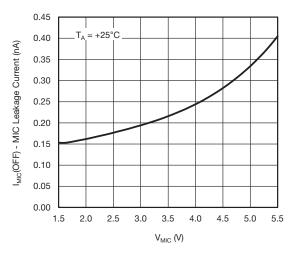
Ear Jack In Current vs.Temperature



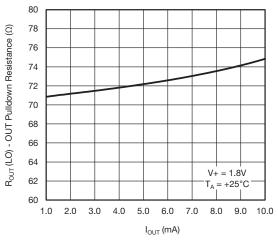
MIC On Resistance vs. Temperature



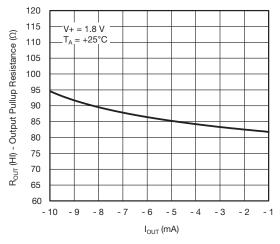
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



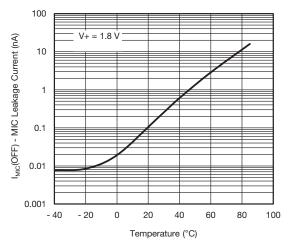
MIC Leakage Current vs. V_{MIC}



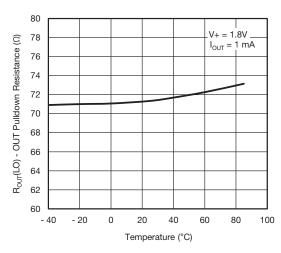
OUT Pulldown Resistance vs. IOUT



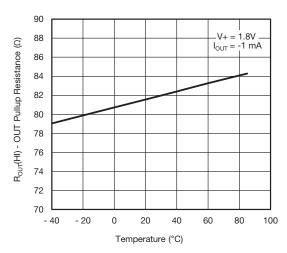
OUT Pullup Resistance vs. IOUT



MIC Leakage Current vs. Temperature



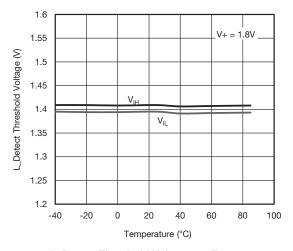
OUT Pulldown Resistance vs. Temperature



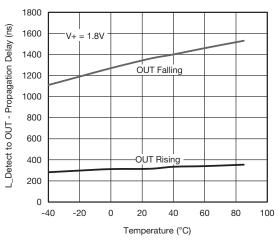
OUT Pullup Resistance vs. Temperature



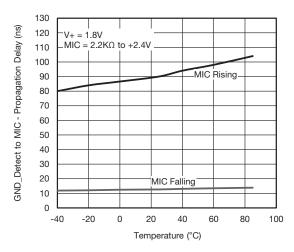
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



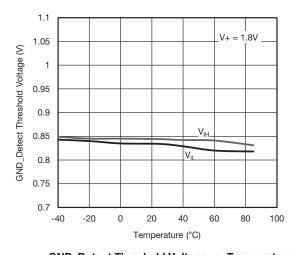
L_Detect Threshold Voltage vs. Temperature



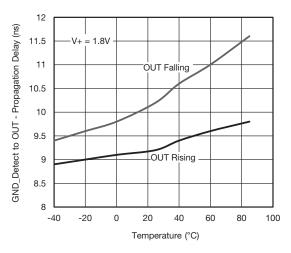
L_Detect to OUT Propagation Delay vs. Temperature



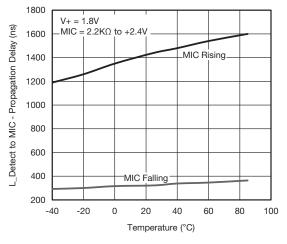
GND_Detect to MIC Propagation Delay vs. Temperature



GND_Detect Threshold Voltage vs. Temperature



GND_Detect to OUT Propagation Delay vs. Temperature



L_Detect to MIC Propagation Delay vs. Temperature

TEST CIRCUIT

Fig. 4 - Test Circuit

TIMING DIAGRAM

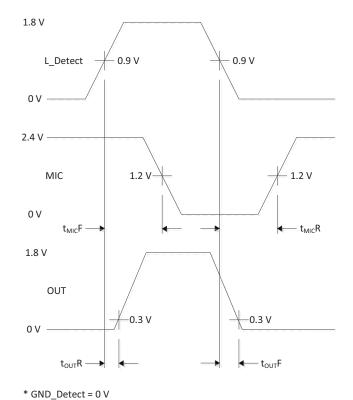
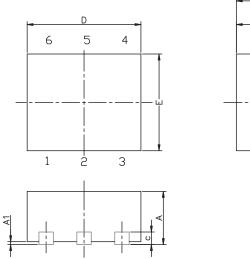


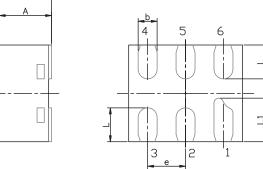
Fig. 5 - Timing Diagram





MINI QFN-6L CASE OUTLINE





DIM.	MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А	0.50	0.55	0.60	0.0197	0.0217	0.0236	
A1	0	-	0.05	0	-	0.002	
b	0.15	0.20	0.25	0.006	0.008	0.010	
С		0.15 ref.			0.006 ref.		
D	1.15	1.20	1.25	0.045	0.047	0.049	
E	0.95	1.00	1.05	0.037	0.039	0.041	
е		0.40 BSC			0.016 BSC		
L	0.30	0.35	0.40	0.012	0.014	0.016	
L1	0.40	0.45	0.50	0.016	0.018	0.020	

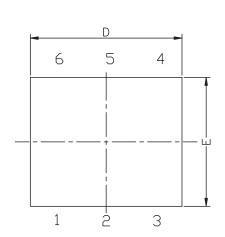
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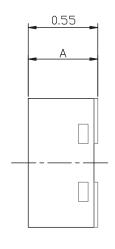
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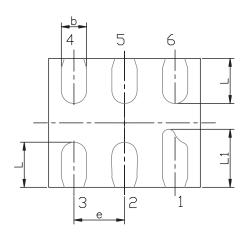


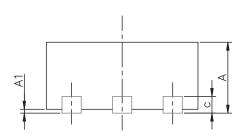


MINI QFN-6L CASE OUTLINE









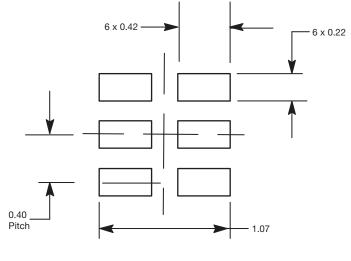
DIM	MILLIMETERS			INCHES			
DIIVI	MIN.	NAM.	MAX.	MIN.	NAM.	MAX.	
Α	0.50	0.55	0.60	0.0197	0.0217	0.0236	
A1	0.00	-	0.05	0.000	1	0.002	
b	0.15	0.20	0.25	0.006 0.008 0.010			
С		0.15 REF		0.006 REF			
D	1.15	1.20	1.25	0.045	0.047	0.049	
Е	0.95	1.00	1.05	0.037	0.039	0.041	
е	0.40 BSC				0.016 BSC		
L	0.30	0.35	0.40	0.012	0.014	0.016	
L1	0.40	0.45	0.50	0.016	0.018	0.020	

ECN T-07039-Rev. A, 12-Feb-07 DWG: 5958



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RECOMMENDED MINIMUM PADS FOR MINI QFN 6L



Mounting Footprint Dimensions in mm



Legal Disclaimer Notice

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Revision: 02-Oct-12 Document Number: 91000