WPMDU1251501 / 171021501

MagI³C Power Module

VDRM - Variable Step Down Regulator Module

7 - 50V / 2.5A / 2.5 - 15V Output

DESCRIPTION

The VDRM series of the MagI³C Power Module family provide a fully integrated DC-DC power supply including the buck switching regulator and inductor in a package.

The WPMDU1251501 offers high efficiency and delivers up to 2.5A of output current. It operates from 7V input voltage up to 50V. It is designed for fast transient response.

It is available in a standard industrial high power density BQFN-41 (9 x 11 x 2.8mm) package with good thermal performance.

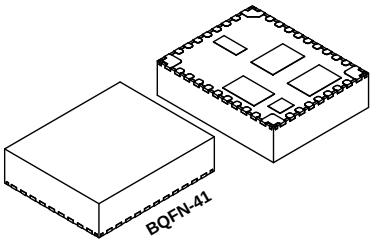
The VDRM regulators have an on-board protection circuitry to guard against thermal overstress and electrical damage featuring thermal shutdown, over-current, short-circuit, overvoltage and undervoltage protections.

FEATURES

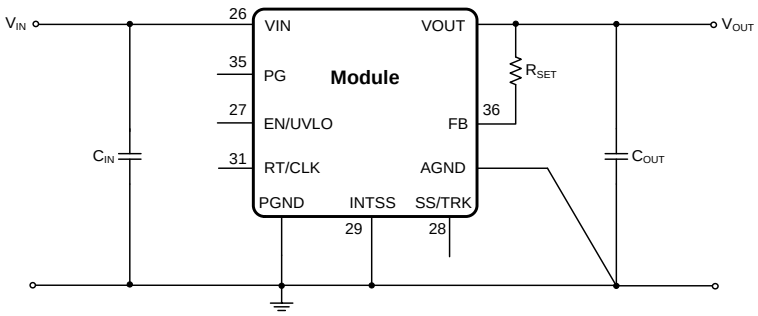
- Peak efficiency up to 96%
- Current capability up to 2.5A
- Wide input voltage range: 7V to 50V
- 65V transients capability
- Output voltage range: 2.5V to 15V
- Continuous output power: 37.5W
- Integrated shielded inductor solution for quick time to market and ease of use
- Adjustable switching frequency (0.3 to 1MHz)
- Current Mode Control
- Undervoltage lockout protection (UVLO)
- Adjustable soft-start and voltage tracking
- Frequency synchronization with external clock
- Thermal shutdown and output short circuit protection
- Cycle by cycle current limit
- Power Good
- Operating ambient temperature up to 85°C
- Operating junction temp. range: -40 to 105°C
- RoHS & REACH compliant
- Mold compound UL 94 Class V0 (flammability testing) certified
- Complies with EN 55022 class B radiated and conducted emissions standard

TYPICAL APPLICATIONS

- Point-of-Load DC-DC applications from 12V and 24V industrial rails
- Industrial, Test & Measurement, Medical applications
- System power supplies
- DSPs, FPGAs, MCUs and MPUs supply
- I/O interface power supply



TYPICAL CIRCUIT DIAGRAM



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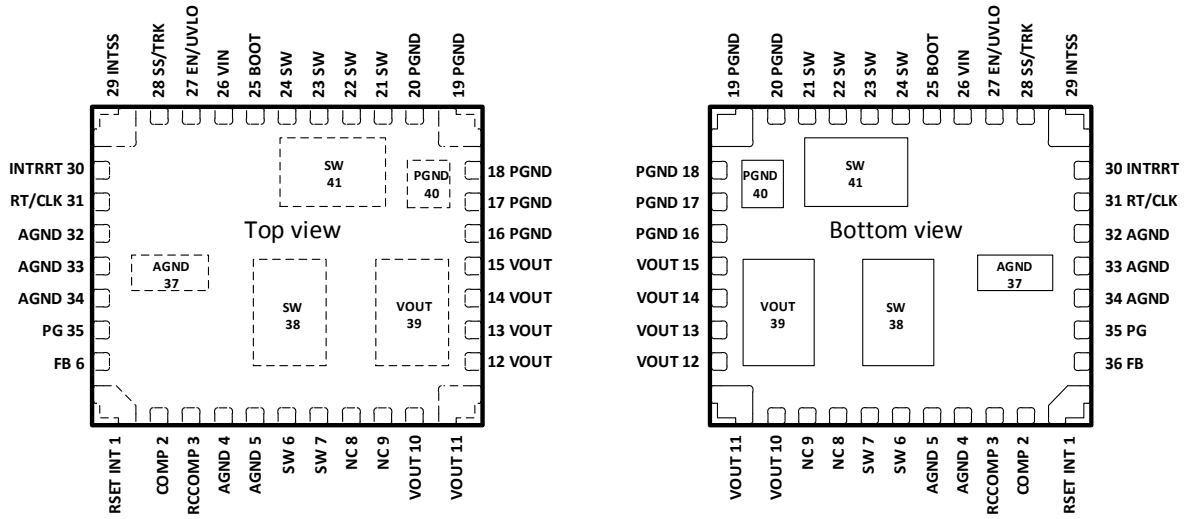
PACKAGE



PIN DESCRIPTION

SYMBOL	PIN	TYPE	PIN DESCRIPTION
VIN	26	Power	The supply input pin is a terminal for an unregulated input voltage source. It is required to place the input capacitor nearby the VIN pin and PGND.
VOUT	10, 11, 12, 13, 14, 15, 39	Power	The output voltage pins are connected to the internal inductor. Connect external bypass capacitors between these pins and PGND.
PGND	16, 17, 18, 19, 20, 40	Power	This is the return current path for the power stage of the device. Connect these pins to the load and to the bypass capacitors associated with VIN and VOUT. Pad 40 should be connected to PCB ground planes using multiple vias for good thermal performance.
AGND	4, 5, 32, 33, 34, 37	Supply	These pins are connected to the internal analog ground (AGND) of the device. This node should be treated as the zero volt ground reference for the analog control circuitry. Pad 37 should be connected to PCB ground planes using multiple vias for good thermal performance. Not all pins are connected together internally. All pins must be connected together externally with a copper plane. Connect AGND to PGND at a single point (at the ground terminal of the first output capacitor). See Layout section for recommendations.
RSET INT	1	Analog	An internal resistor of 10KΩ is connected internally between $R_{SET\ INT}$ and FB. This is the low side resistor of the feedback voltage divider. Must be connected to AGND.
FB	36	Input	Connect a resistor from the last output capacitor terminal to FB to set the output voltage.

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PINS FOR OPTIONAL USE

SYMBOL	PIN	TYPE	PIN DESCRIPTION
EN/UVLO	27	Input	Enable and UVLO adjust pin. Use an open drain or open collector logic device to ground this pin to disable the device. A resistor divider between this pin, AGND, and VIN sets the UVLO voltage.
RT/CLK	31	Input	This pin sets the switching frequency. Left open will set the internal oscillator to the default switching frequency. An external resistor from this pin to AGND sets a user defined switching frequency. This pin can also be used to synchronize with an external clock.
INTRRT	30	Analog	Internal Resistor ($R_{RT\ INT}$) which defines the default switching frequency. Must be connected to AGND.
SS/TRK	28	Input	Soft-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage rise time during start-up. A voltage applied to this pin allows for tracking and sequencing control.
INTSS	29	Input	Internal soft-start or track feature select. Connect this pin to AGND to enable the internal SS capacitor. Leave this pin open to enable the tracking feature of pin SS/TRK.
PG	35	Output	Power Good flag pin. This open drain output asserts low if the output voltage is more than approximately ±6% out of regulation. A pull-up resistor is required if this function is used.

AUXILIARY PINS DESCRIPTION

SYMBOL	PIN	TYPE	PIN DESCRIPTION
COMP	2	Output	Output of the error amplifier. Do Not Connect. This pin must be soldered to an isolated pad.
RCCOMP	3	Analog	Internal R and C of the compensation network. Do Not Connect. This pin must be soldered to an isolated pad.
BOOT	25	Supply	Internal bootstrap pin for the high-side MOSFET. Do Not Connect. This pin must be soldered to an isolated pad.
SW	6, 7, 21, 22, 23, 24, 38, 41	Power	Switch node. Do not place any external component on these pins or tie them to a pin of another function.
NC	8, 9	Not connect.	These pins are not connected to the internal circuitry, and are not connected to each other.

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ORDERING INFORMATION

ORDER CODE	PART DESCRIPTION	SPECIFICATIONS	PACKAGE	PACKING UNIT
171021501	WPMDU1251501NT	2.5A / 37.5W version	BQFN-41	Tape and Reel with 250 Units
178021501	Evaluation Board	2.5A / 37.5W version		1

PACKAGE SPECIFICATIONS

Weight	Molding compound	UL class	Certificate number
0.54g	EME-G770H	UL94 V-0	E41429

SALES INFORMATION

SALES CONTACTS
Würth Elektronik eiSos GmbH & Co. KG EMC & Inductive Solutions Max-Eyth-Str. 1 74638 Waldenburg Germany Tel. +49 (0) 79 42 945 - 0 www.we-online.com powermodules@we-online.com

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ABSOLUTE MAXIMUM RATINGS

Caution:
Exceeding the listed absolute maximum ratings may affect the device negatively and may cause permanent damage.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
VIN	Input voltage	-0.3	65	V
VOUT	Output voltage	-0.6	V_{IN}	V
AGND	AGND to PGND	-0.2	2.3	V
SW	Switching node pin voltage	-0.6	65	V
	Switching node pin voltage (10ns transient)	-2	65	V
EN/UVLO	Enable/Undervoltage lockout pin voltage	-0.3	5	V
	Enable/Undervoltage lockout pin source current		100	µA
FB	Output voltage adjust pin voltage	-0.3	3	V
PG	Power good pin voltage	-0.3	6	V
	Power good pin sink current		10	mA
SS/TRK	Soft-start/Tracking pin voltage	-0.3	3	V
	Soft-start/Tracking pin sink current		200	µA
INTSS	Internal soft-start or tracking feature select pin voltage	-0.3	3	V
RT/CLK	Timer/Clock pin voltage	-0.3	3.6	V
	Timer/Clock pin source current		100	µA
$T_{storage}$	Assembled, non operating storage temperature	-65	150	°C
T_{SOLR}	Peak case/leads temperature during reflow soldering, max. 30sec per JEDEC J-STD020. Maximum three cycles!		245 ±5°C	°C
Mechanical Shock	Mil-STD-883D, Method 2002.3, 1msec, ½ sine, mounted		1500	G
Mechanical Vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz		20	G

OPERATING CONDITIONS

Operating conditions are conditions under which operation of the device is intended to be functional. All values are referenced to GND.

SYMBOL	PARAMETER	MIN (1)	TYP (2)	MAX (1)	UNIT
V_{IN}	Input voltage	7	-	50	V
V_{OUT}	Regulated output voltage	2.5		15	V
f_{SW}	Switching frequency	300	-	1000	kHz
T_A	Ambient temperature range	-40	-	85 (3)	°C
T_J	Junction temperature range	-40	-	105	°C
I_{OUT}	Nominal output current			2.5	A

THERMAL SPECIFICATIONS

SYMBOL	PARAMETER	TYP	UNIT
θ_{JA}	Thermal resistance junction to ambient (4)	14	°C/W
ϕ_{JT}	Thermal resistance junction to top (5)	3.3	°C/W
ϕ_{JB}	Thermal resistance junction to board (6)	6.8	°C/W
T_{SD}	Thermal shutdown, junction temperature, rising	180	°C
	Thermal shutdown hysteresis, falling	15	°C

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ELECTRICAL SPECIFICATIONS

MIN and MAX limits are valid for the recommended **ambient** temperature range of **-40°C to 85°C**. Typical values represent statistically the utmost probability at following conditions: V_{IN} = 24 V, V_{OUT} = 5.0 V, I_{OUT} = 2.5 A, RT = Open, C_{IN} = 2 x 2.2 µF ceramic, C_{OUT} = 2 x 47 µF ceramic, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
Output current						
I_{OCP}	Over current protection		-	5.1	-	A
Accuracy						
V_{FB}	Reference accuracy	T_A = 25°C; I_{OUT} = 100mA with internal feedback resistor	-	-	±2.0 (7)	%
	Temperature variation	-40°C ≤ T_A ≤ +85°C	-	±0.5	±1.0	%
V_{OUT}	Line regulation	Over input voltage range	-	±0.1	-	%
	Load regulation	Over output current range	-	±0.4	-	%
	Total output voltage variation	Includes set-point, line, load, and temperature variation	-	-	±3.0 (7)	%
	Output voltage ripple	0.25A ≤ I_{OUT} ≤ 2.5A, V_{OUT} ≥3.3V	-	1	-	% of V_{OUT}
Switching frequency						
f_{SW}	Free-running oscillator frequency	RT/CLK pin open	300	400	500	kHz
f_{CLK}	Synchronization clock frequency range		300	-	1000	kHz
D_{CLK}	Synchronization clock duty cycle range		25	50	75	%
V_{CLK-H}	High-level threshold CLK	Relative to AGND	-	1.9	2.2	V
V_{CLK-L}	Low-level threshold CLK	Relative to AGND	0.5	0.7	-	V
Enable and undervoltage lockout						
V_{UVLO}	V_{IN} undervoltage lockout	No hysteresis, rising and falling	-	2.5	-	V
V_{EN}	EN threshold trip point	V_{EN} rising and falling, no hysteresis	1.15	1.25	1.36 (8)	V
I_{EN}	EN input current	V_{EN} < 1.15V	-	-0.9	-	µA
		V_{EN} > 1.36 V	-	-3.8	-	µA
		I_{EN} to AGND, V_{EN}= 0V	-	1.3	4	µA
Power Good						
PG	Power good thresholds	V_{OUT} rising, V_{OUT} GOOD	-	94	-	%
		V_{OUT} rising, V_{OUT} FAULT	-	109	-	%
		V_{OUT} falling, V_{OUT} GOOD	-	91	-	%
		V_{OUT} rising, V_{OUT} FAULT	-	106	-	%
	Power good low voltage	I(PG) = 3.5mA	-	0.2	-	V
Efficiency						
η	Efficiency	V_{IN} = 24V, I_{OUT} = 1.5 A, V_{OUT} = 5 V, f_{SW} = 500 kHz	-	84	-	%
		V_{IN} = 48V I_{OUT} = 1.5A, V_{OUT} = 5V, f_{SW} = 500 kHz	-	79	-	%

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SYMBOL	PARAMETER	TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
Transient Response						
T_{TR}	Transient response Recovery time	1A/µs load step from 50 to 100%,	-	400	-	µs
V_{TR}	Transient response V_{OUT} over/undershoot	1A/µs load step from 50 to 100%,	-	90	-	mV
Quiescent current						
I_Q	Input quiescent current	EN = 0V, T_A = 25°C, 3.5V ≤ V_{IN} ≤ 60V		1.3	4	µA
		Non switching: V_{FB} = 0.83V, T_A = 25°C, V_{IN} = 12 V		200		µA

RELIABILITY

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
MTBF	Mean Time Between Failures	Confidence level 60%, T_A=55°C, Activation energy 0.7eV, 1000 hrs test duration, 46185 samples, 1 fail		$1.79 \cdot 10^9$		h

NOTES

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

(2) Typical numbers are valid at 25°C ambient temperature and represent statistically the utmost probability assuming the Gaussian distribution.

(3) Depending on heat sink design, number of PCB layers, copper thickness and air flow.

(4) Measured on a 100 x 100mm four layer board, with 35µm (1 ounce) copper, no air flow

(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature, TJ, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JT} * Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.

(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} * Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

(7) The stated limit of the feedback voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor $R_{SET\ INT}$. The overall output voltage tolerance is affected by the tolerance of the external R_{SET} resistor.

(8) Value when no voltage divider is present at the EN/UVLO pin.

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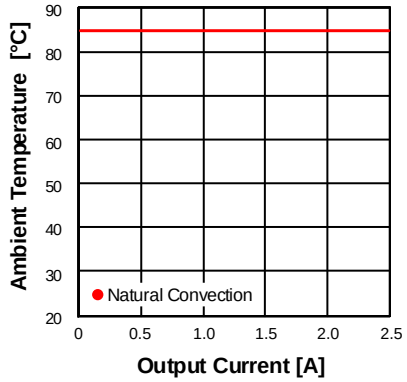
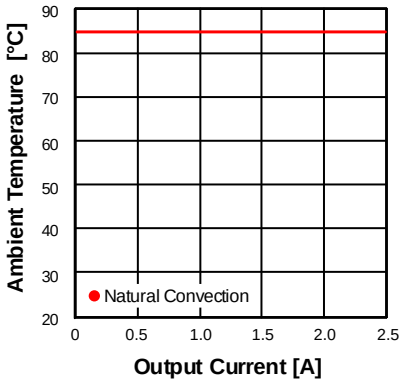
TYPICAL PERFORMANCE CURVES

If not otherwise specified, the following conditions apply: V_{IN} = 7-50V; C_{IN} = 2x 2.2µF X7R ceramic; C_O = 2x 47µF X7R ceramic, T_{AMB} = 25°C.

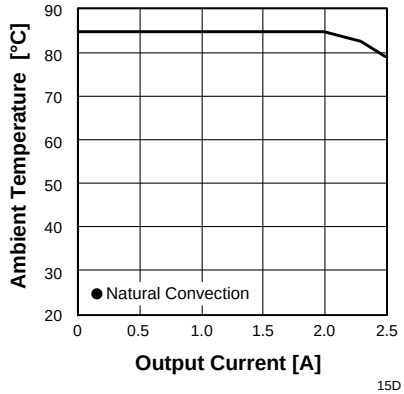
Thermal Derating: V_{IN} = 12V; V_{OUT} = all voltages



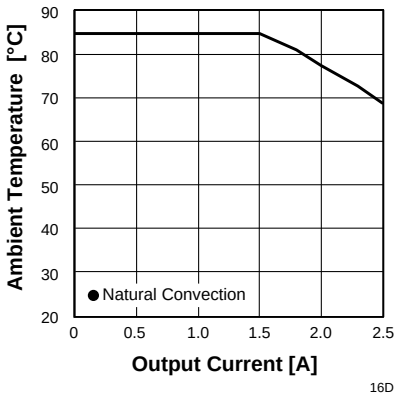
Thermal Derating: V_{IN} = 24V; V_{OUT} = all voltages



Thermal Derating: V_{IN} = 36V; V_{OUT} = all voltages



Thermal Derating: V_{IN} = 48V; V_{OUT} = all voltages



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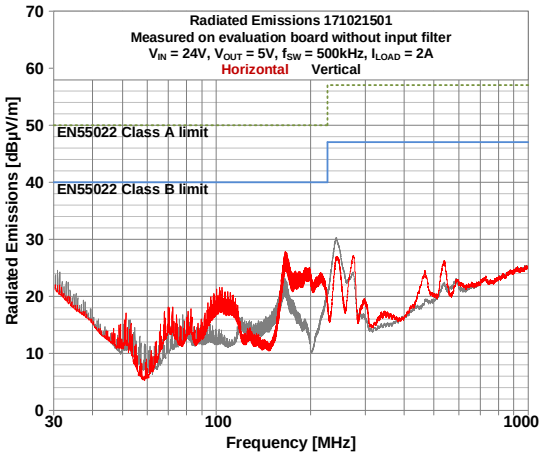
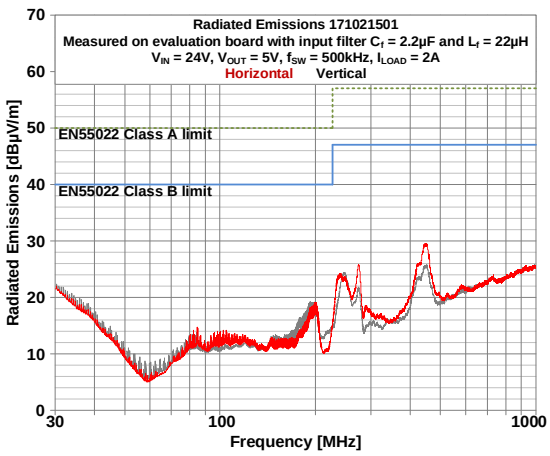
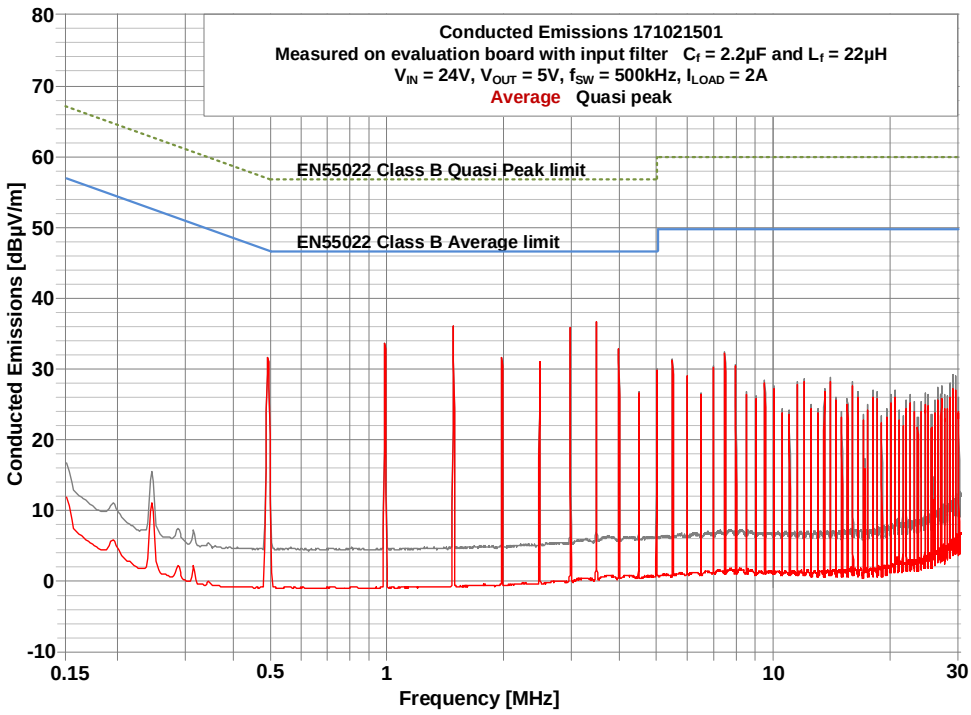
TYPICAL PERFORMANCE CURVES

If not otherwise specified, the following conditions apply: V_{IN} = 7-50V; C_{IN} = 2x 2.2µF X7R ceramic; C_O = 2x 47µF X7R ceramic, T_{AMB} = 25°C.







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TYPICAL PERFORMANCE CURVES

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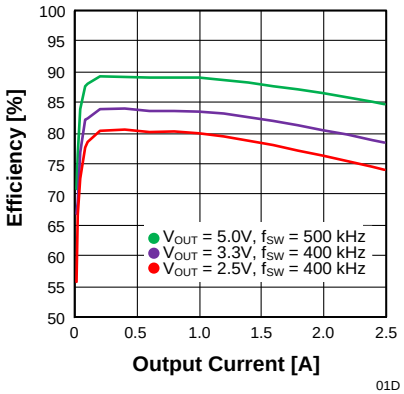
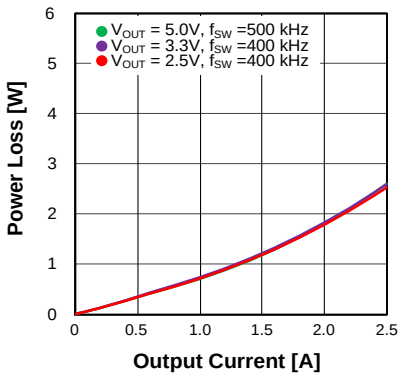
Efficiency: V_{IN} = 12V @ T_{AMB} = 25°C



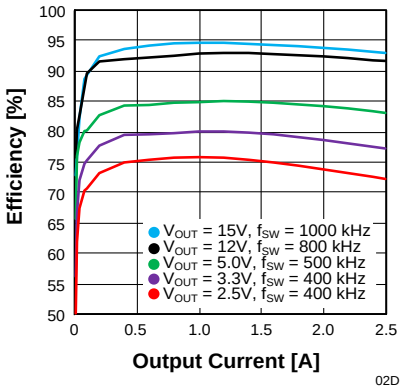
01D

Power Loss: V_{IN} = 12V @ T_{AMB} = 25°C



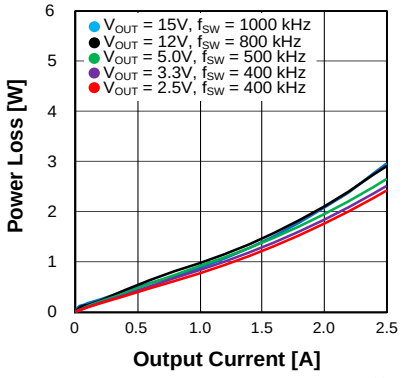
05D

Efficiency: V_{IN} = 24V @ T_{AMB} = 25°C



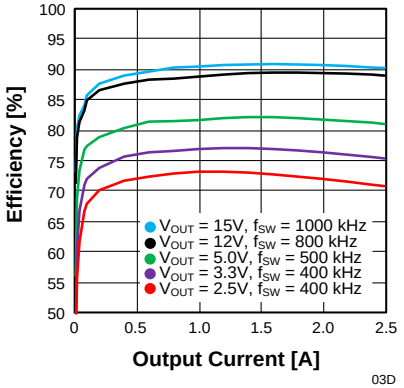
02D

Power Loss: V_{IN} = 24V @ T_{AMB} = 25°C



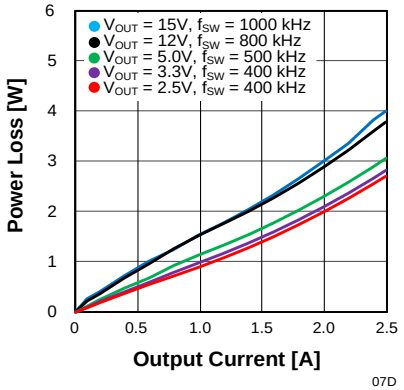
06D

Efficiency: V_{IN} = 36V @ T_{AMB} = 25°C



03D

Power Loss: V_{IN} = 36V @ T_{AMB} = 25°C



07D

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TYPICAL PERFORMANCE CURVES

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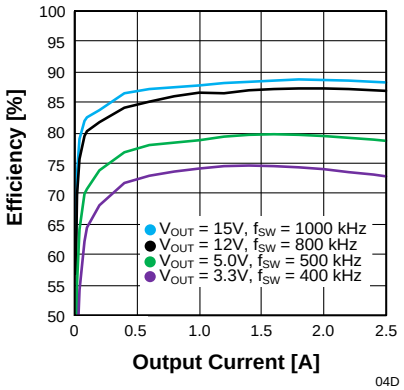
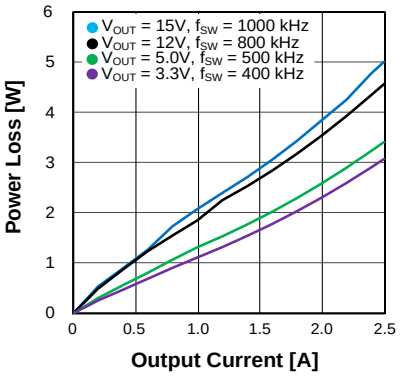
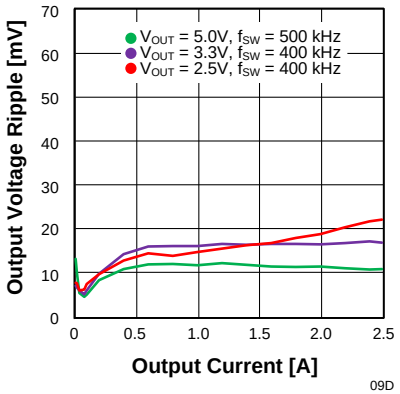
Efficiency: V_{IN} = 48V @ T_{AMB} = 25°C



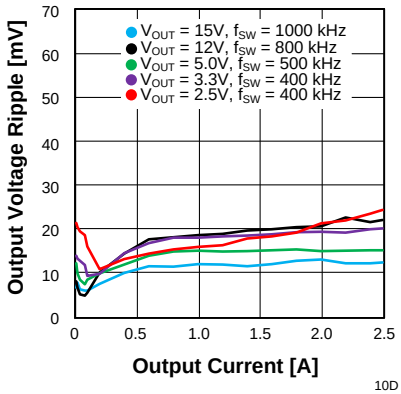
Power Loss: V_{IN} = 48V @ T_{AMB} = 25°C



Output Voltage Ripple: V_{IN} = 12V @ T_{AMB} = 25°C



Output Voltage Ripple: V_{IN} = 24V @ T_{AMB} = 25°C



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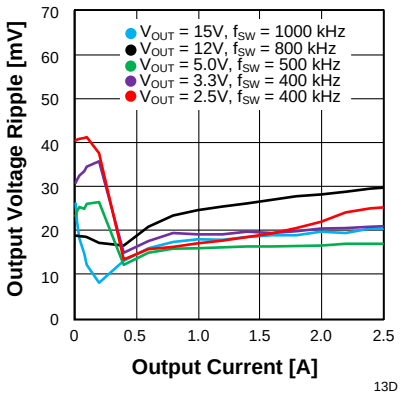

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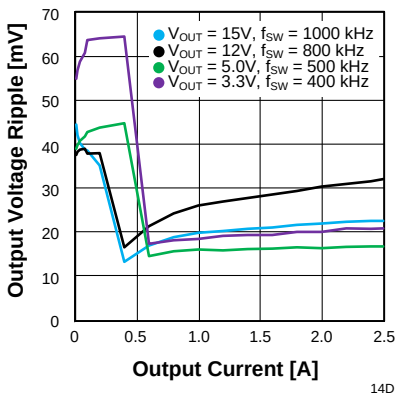

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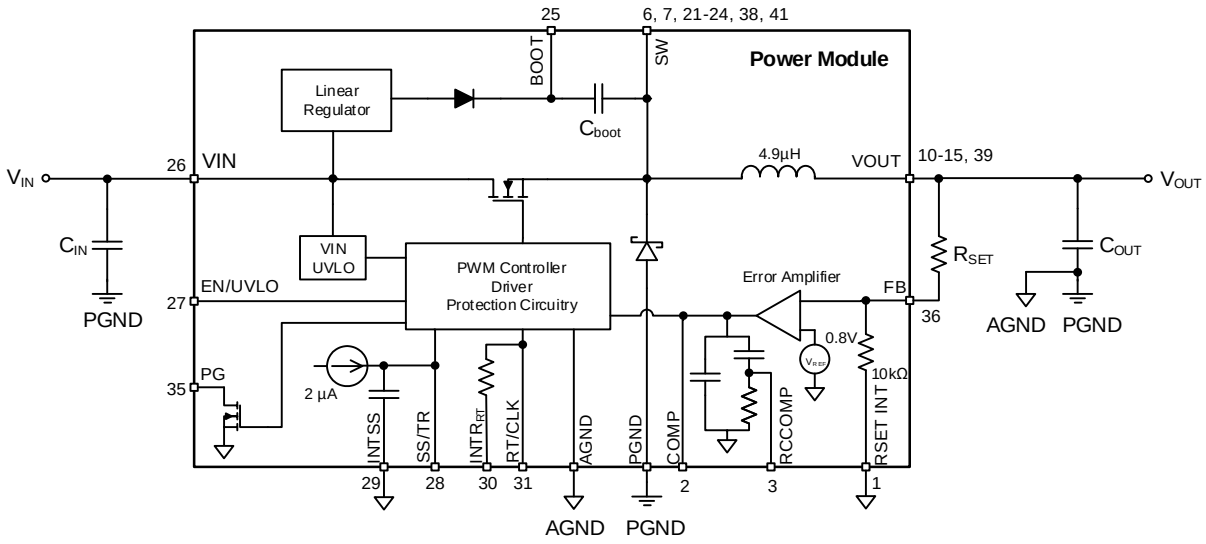
BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The MagI³C Power Module WPMDU1251501 is based on a non synchronous step down regulator with integrated MOSFET, schottky diode and a power inductor. The control scheme is based on a Current Mode (CM) regulation loop.

The V_{OUT} of the regulator is divided with the feedback resistor network R_{SET} and an internal 10KΩ resistor and fed into the error amplifier which compares this signal with the internal 0.8V reference V_{REF}. The error signal is amplified and controls the on-time of a fixed frequency pulse with generator. This signal drives the power MOSFET.

The Current Mode architecture features a constant frequency during load steps. Only the on-time is modulated. It is internally compensated and stable with low ESR output capacitors and requires no external compensation network.

This architecture supports fast transient response and very small output ripple values (less than 10mV) are achieved.

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DESIGN FLOW

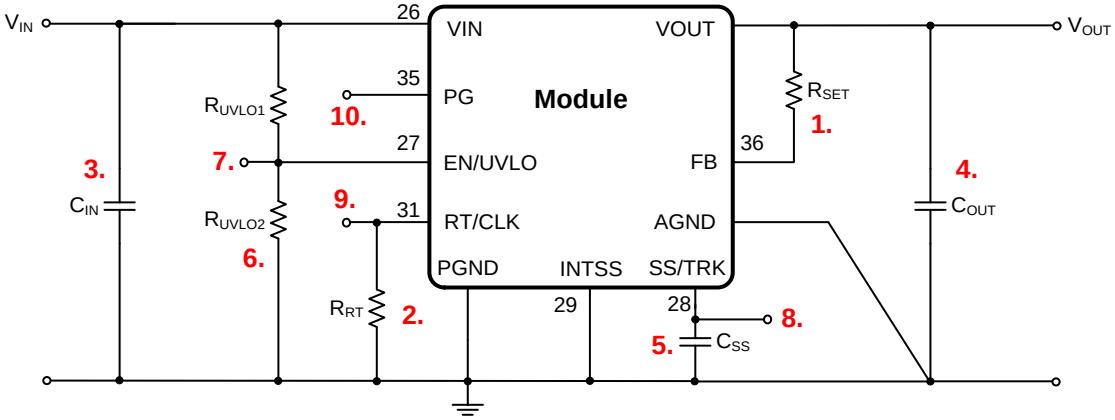
The next 10 simple steps will show how to select the external components to design your power application.

Essential Steps

1. Set output voltage
2. Set operating frequency
3. Select input capacitor
4. Select output capacitor

Optional Steps

5. Select soft-start capacitor
6. Select undervoltage lockout divider
7. Enable/Disable
8. Voltage tracking
9. Synchronization to an external clock
10. Power Good



Step 1 Setting the output voltage (V_{OUT})

The MagI³C Power Module is designed to provide output voltages from 2.5 V to 15 V. The output voltage is determined by the value of R_{SET}, which must be connected between the V_{OUT} node and the FB pin (Pin 36). For output voltages higher than 5 V, improved operating performance can be obtained by increasing the operating frequency. This adjustment requires the addition of R_{RT} between RT/CLK (Pin 31) and AGND (Pin 30). See the Step 2 Set operating frequency section for more details. Table 1 gives the standard external R_{SET} resistor for a number of common bus voltages and also includes the recommended R_{RT} resistor for output voltages above 5 V.

V_{OUT}	R_{SET}
2.5V	21.5kΩ
3.3V	31.6kΩ
5V	52.3kΩ
9V	102kΩ
12V	140kΩ
15V	178kΩ

Table 1: Recommended standard output voltages

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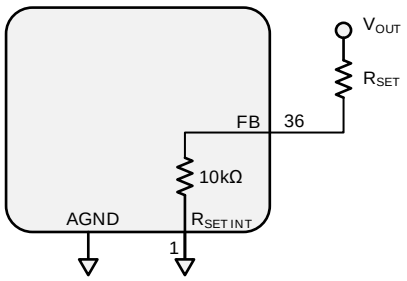
For other output voltages the value of R_{SET} can be calculated using the following formula.

$$R_{SET} = 10 * \left(\frac{V_{OUT}}{0.798} - 1\right) \text{ k}\Omega \qquad (1)$$

The MagI³C Power Module operates over the input voltage range of 7 V to 50 V. For reliable start-up and operation at light loads, the minimum input voltage depends on the output voltage (see table below).

Output voltage range	Condition	Input voltage
V_{OUT} ≤ 12V	7V ≤ V_{IN} ≤ 50V	V_{INmin} ≥ V_{OUT} + 3V
		V_{INmax} ≤ V_{OUT} *15
V_{OUT} > 12V		V_{INmin} ≥ V_{OUT} *1.33
		V_{INmax} ≤ V_{OUT} *15

Although the device can safely handle input surge voltages up to 65 V, sustained operation at input voltages above 50 V is not recommended. See the Step 6 (Undervoltage Lockout (UVLO) Threshold section) for more information.



Step 2 Setting the operating frequency (f_{SW})

Nominal switching frequency of the MagI³C Power Module is set from the factory at 400 kHz. This switching frequency is optimized for output voltages below 5 V. For output voltages of 5 V and above, better operating performance can be obtained by raising the operating frequency. This is easily done by adding a resistor, R_{RT} from the RT/CLK pin (Pin 31) to the AGND pin (Pin 30). Raising the operating frequency reduces output voltage ripple, lowers the load current threshold where pulse skipping begins, and improves transient response. The recommended switching frequency for typical output voltages is listed in Table 2.
For the maximum recommended output voltage value of 15 V, the switching frequency computes to 1 MHz. Operation above 1 MHz is not recommended.

V_{OUT}	f_{SW}	R_{RT}
2.5V	**400kHz**	Open
3.3V	**400kHz**	Open
5V	**500kHz**	1,1MΩ
9V	**700kHz**	365kΩ
12V	**800kHz**	267kΩ
15V	**1MHz**	178kΩ

Table 2: Standard Switching Frequencies

It is also possible to synchronize the switching frequency to an external clock signal. See the Step 8.Synchronization CLK option section for further details. While it is possible to set the operating frequency higher than 400 kHz when using the device at output voltages of 5 V or less, minimum duty cycle and pulse skipping issues restrict the maximum recommended input voltage under these conditions. The recommended operating conditions for the MagI³C Power Module can be summarized by Figure 1. The graph shows the maximum input voltage vs. output voltage restriction for several operating frequencies. The lower boundary of the graph shows the minimum input voltage as a function of the output voltage.

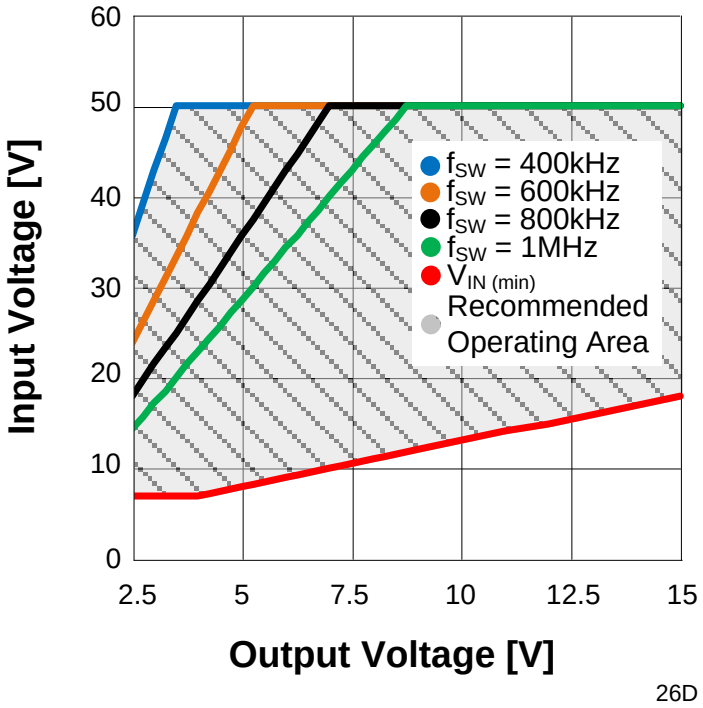


Figure 1. Input Voltage vs. Output Voltage Operating Area

Step 3 Select input capacitor (C_{IN})

The WPMDU1251501 MagI³C power module contains no internal input capacitors. Therefore an external input capacitance placed directly at the V_{IN} pin is required to handle the input ripple current of the application. The input capacitor can be several capacitors in parallel. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Input ripple current rating is dictated by the equation:

$$I_{C_{INRMS}} \approx \frac{1}{2} * I_{OUT} * \sqrt{\frac{D}{1-D}} \quad (2) \quad \text{where} \quad D \approx \frac{V_{OUT}}{V_{IN}}$$

(As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 * V_{OUT}$).

Recommended minimum input capacitance is 4.4µF X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. It is also recommended that attention be paid to the voltage and temperature deratings of the capacitor selected. It should be noted that ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this rating.

If the system design requires a certain minimum value of peak-to-peak input ripple voltage (ΔV_{IN}) be maintained then the following equation may be used.

$$C_{IN} \geq \frac{I_{OUT} * D * (1-D)}{f_{SW} * \Delta V_{IN}} \quad (3)$$

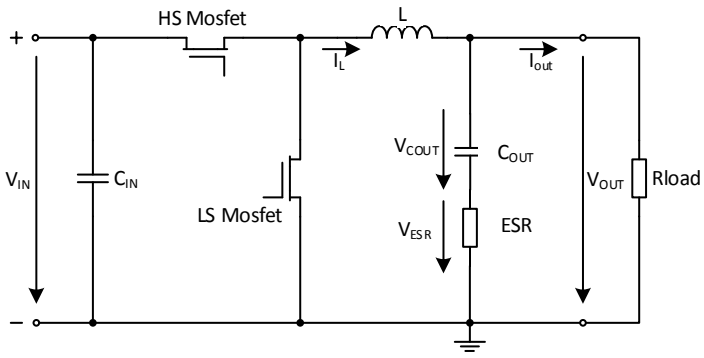
If ΔV_{IN} is 1% of V_{IN} for a 24V input to 5V output application this equals 240 mV and f_{SW} = 500kHz.

$$C_{IN} \geq \frac{2.5A * \frac{5V}{24V} * (1-\frac{5V}{24V})}{500000 * 0.24V}$$

$$C_{IN} \geq 3.4\mu F$$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

Step 4 Select output capacitor (C_{OUT})



None of the required output capacitors is integrated within the module. . At a minimum, the output capacitor must meet the worst case RMS current rating of $0.5 * \Delta I_L$, as calculated in equation (4).

$$\Delta I_L = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{f_{SW} * L * V_{IN}} \quad (4)$$

Beyond that, additional capacitance will reduce output ripple as long as the ESR is low enough to permit it. There is no limit of the maximum output capacitance. Please consider the derating of the nominal capacitance value due to temperature, aging and applied DC voltage (only for MLCC, e.g. X7R up to -50%).

Selection by output voltage ripple requirements

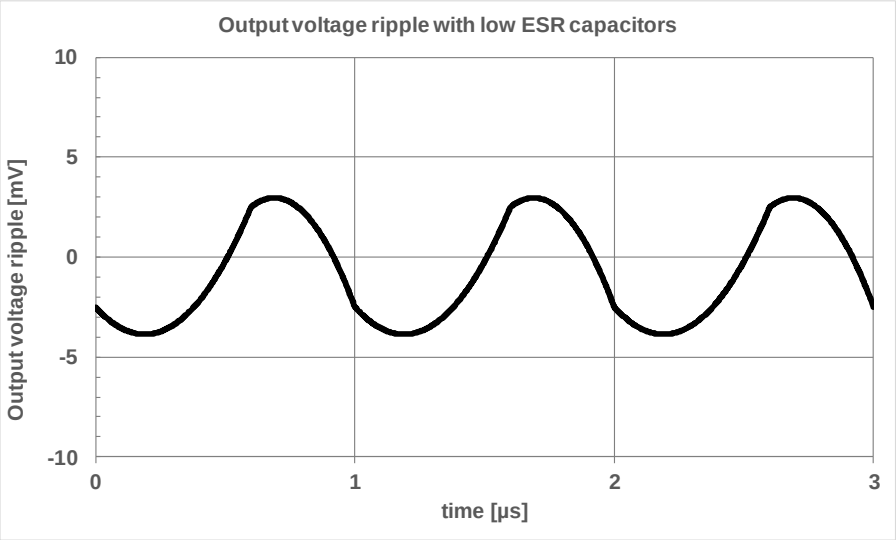
The capacitor should be selected in order to minimize the output voltage ripple and provide a stable voltage at the output. Under steady state conditions, the voltage ripple observed at the output can be defined as:

$$V_{OUT\,ripple} = \Delta I_L * ESR + \Delta I_L * \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}} \quad (5)$$

Very low ESR capacitors, like ceramic and polymer electrolytic, are recommended. If a low ESR capacitor is selected, the equation (4) can be simplified and a first condition for the minimum capacitance value can be derived:

$$C_{OUT} \geq \frac{\Delta I_L}{8 * V_{OUT\,ripple} * f_{SW}} \quad (6)$$

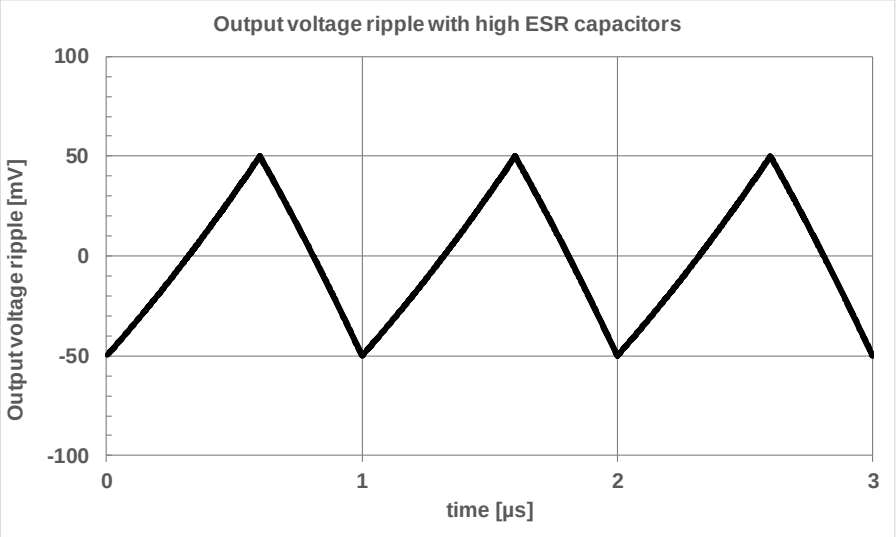
The use of very low ESR capacitors leads to an output voltage ripple as shown below:



When capacitors with slightly higher ESR are utilized, the dominant parameter which influences the output voltage ripple is just the ESR:

$$ESR \leq \frac{V_{OUT\ ripple}}{\Delta I_L} \quad (7)$$

Consequently the shape of the output voltage ripple changes, as shown below:



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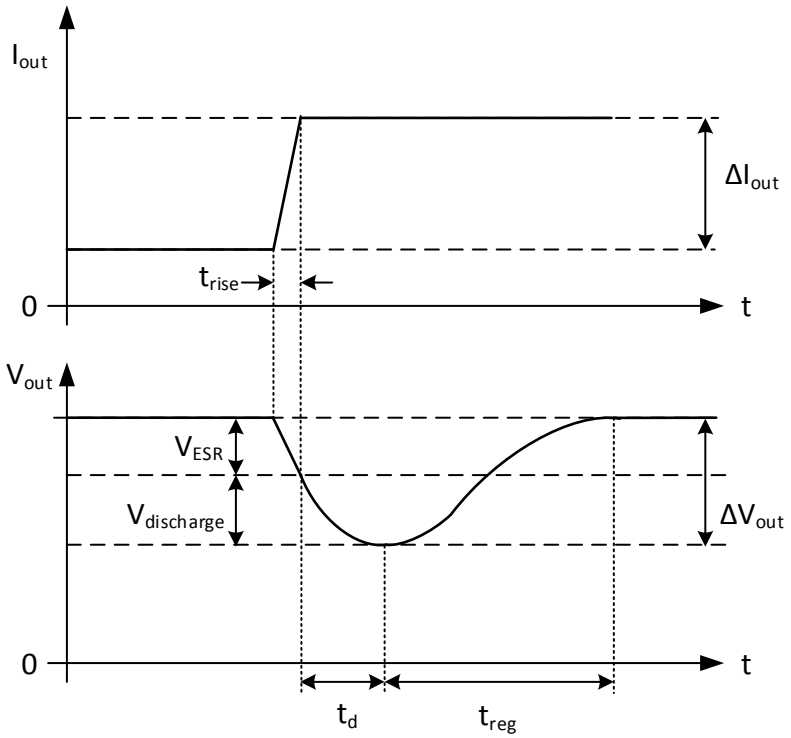
Selection by load step requirements

The output voltage is also affected by load transient (see picture below).
By the output current transition from a low to a high value, the voltage at the output capacitor (V_{OUT}) drops. This involves two contributions. One is caused by the voltage drop across the ESR (V_{ESR}) and depends on the slope of the rising edge of the current step (t_{rise}). For low ESR values and small load currents, this is often negligible. It can be calculated as follows:

$$V_{ESR} = ESR * \Delta I_{OUT} \quad (8)$$

Where ΔI_{OUT} is the load step, as shown in the picture below (simplified: no voltage ripple is shown).



The second component is the voltage drop due to discharge of the output capacitor, which can be estimated as:

$$V_{discharge} = \frac{\Delta I_{OUT} \cdot t_d}{2 \cdot C_{OUT}} \quad (9)$$

In a current mode architecture the t_d is strictly related to the bandwidth of the regulation loop and influenced by the C_{OUT} (increasing C_{OUT}, the t_d increases as well).

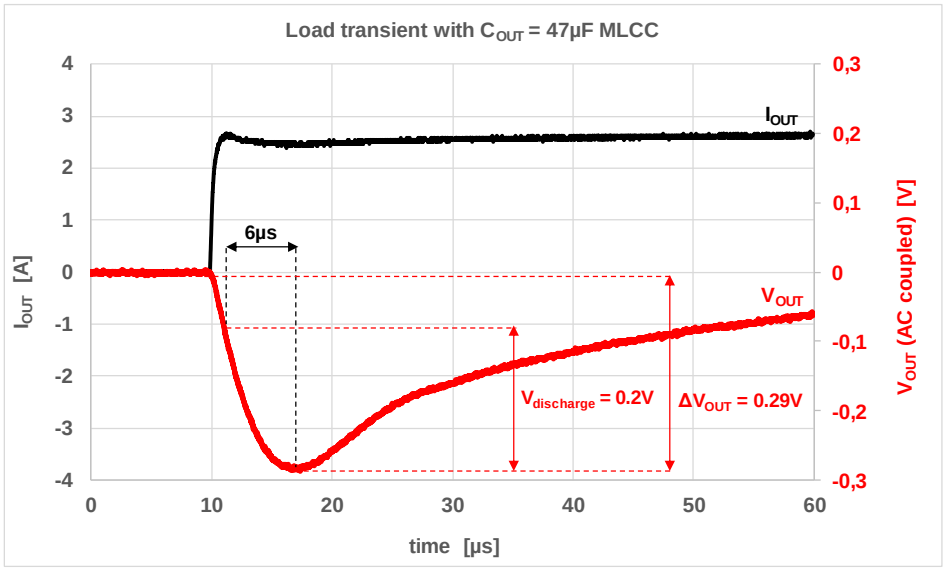
In order to choose the value of the output capacitor, the following steps should be followed:

1. According to the operating conditions (V_{IN}, V_{OUT} and f_{SW}), select the minimum C_{OUT} recommended in table on page 38.
2. Measure t_d.
3. Calculate the appropriate value of C_{OUT} for the maximum voltage drop $V_{discharge}$ allowed at a defined load step, using the following equation (10), derived from equation (9):

$$C_{OUT} \geq \frac{\Delta I_{OUT} \cdot t_d}{2 \cdot V_{discharge}} \quad (10)$$

4. As above mentioned, changing C_{OUT} affects also t_d. Therefore a new measure should be performed and, if necessary, the step 2 and 3 should be repeated (it is an iterative process and few steps could be required).

Example. V_{IN} = 12V, V_{OUT} = 3.3V, ΔI_{OUT} = 2A (from 0.5A to 2.5A), f_{sw} = 400kHz, ΔV_{OUT}<0.1V.
According to the table on page 38, two output MLCC of 47µF would be necessary. After mounting these capacitors, the load transient should be performed and the t_d measured (see picture below).



The ΔV_{OUT} = 0.13V and t_d= 3µs. It is important to remind that the ΔV_{OUT} includes also the voltage drop during t_{rise}, mainly due to the ESR (V_{ESR} = 60mV, see picture above). In order to achieve the desired maximum ΔV_{OUT}, the $V_{discharge}$ should be below 0.025V. Using the equation (9), the minimum required output capacitor is:

$$C_{OUT} \geq \frac{2A \cdot 3\mu s}{2 \cdot 0.025V} = 120\mu F$$

To achieve the calculated value of C_{OUT}, an additional MLCC of 47µF is mounted in parallel.

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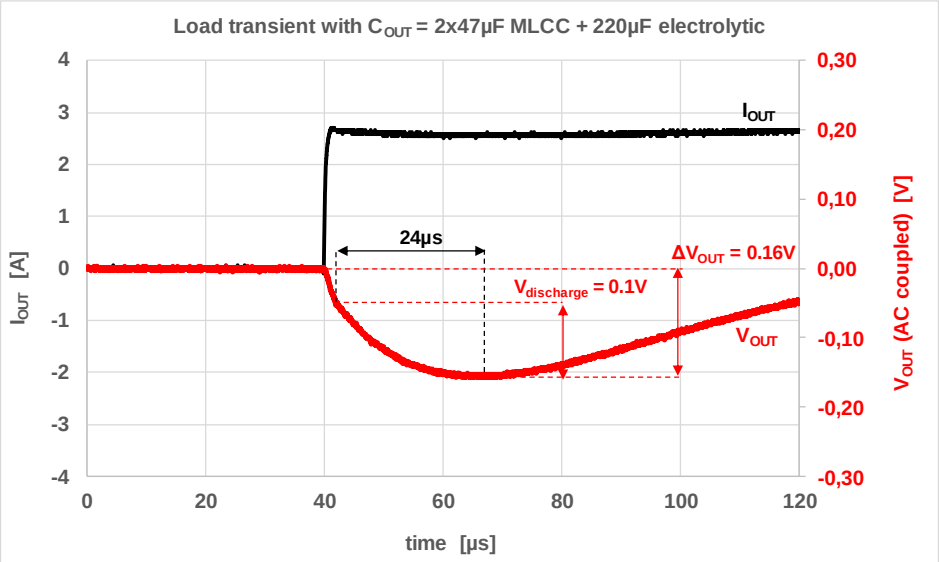
The result with three MLCC of 47µF in parallel is shown below:



In order to have a safer margin from the desired ΔV_{OUT}<0.1V, additional capacitance at output would be required.

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Step 5 Select Soft-Start capacitor (C_{SS})

Programmable soft-start permits the regulator to slowly ramp up to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot.

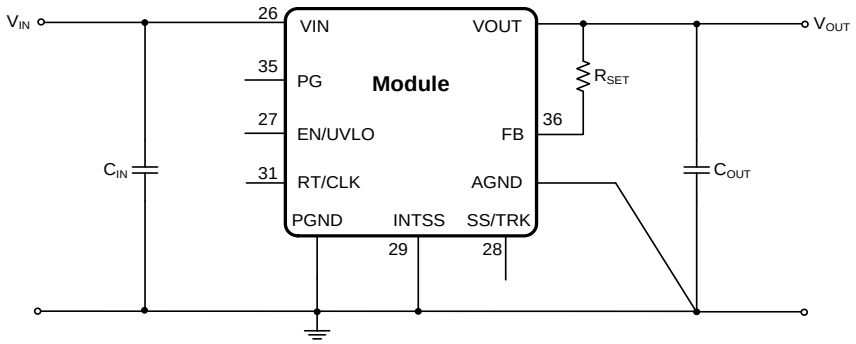

Figure 2. Basic Soft-Start configuration

In minimum external components configuration (Figure 2), connecting the INTSS pin (Pin 29) to AGND while leaving SS pin (Pin 28) the MagI³C Power Module powers-up with a soft-start interval of approximately 5ms, using the internal soft-start circuitry. This reduces the slope of the output voltage. The soft-start circuitry introduces a short time delay when a valid input voltage is recognized.

Figure 3 shows the start-up waveforms of the MagI³C Power Module, operating from a 24 V input and the output voltage adjusted to 5 V.

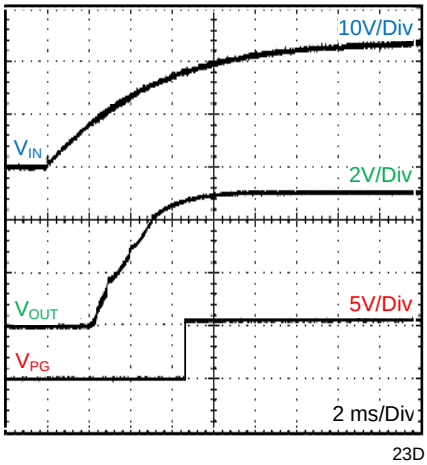

Figure 3. Startup V_{IN}=10V; I_{OUT}=2A

For output voltages of 5 V or less, the soft-start capacitance built into the MagI³C Power Module is sufficient for a turn-on ramp rate that does not induce large surge currents while charging the output capacitors. For output voltages higher than 5 V, an additional soft-start capacitance is recommended. For 12 V to 15 V output voltages, a 22 nF capacitor should be connected between the SS/TRK pin (Pin 28) and AGND, while connecting the INTSS pin (Pin 29) to AGND as well. Figure 4 shows an external SS capacitor connected to the SS pin and the INTSS pin connected to AGND. See Table 3 below for SS capacitor values and timing interval.

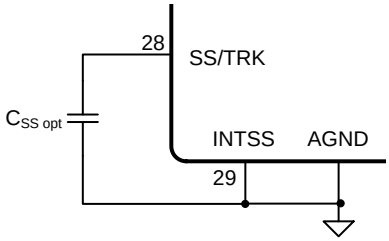

Figure 4. Soft-Start Capacitor Css and INTSS connection

Soft-Start Time t_{SS}	**Capacitor C_{SS}**
5ms	Open
7ms	4.7nF
10ms	10nF
13ms	15nF
17ms	22nF

Table 3: Recommended Soft-Start Capacitors for typical Start times

Step 6 Optional: Program undervoltage lockout divider (R_{UVLO1} and R_{UVLO2})

The function of the R_{UVLO1} and R_{UVLO2} divider is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable external undervoltage lockout.
This is often used in battery powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turn-on of the supply as the main input voltage rail rises at power-up. Most systems will benefit by using the precision Enable threshold to establish a system undervoltage lockout. The recommended approach is to choose an input UVLO level higher than the target regulated output voltage for the stage.

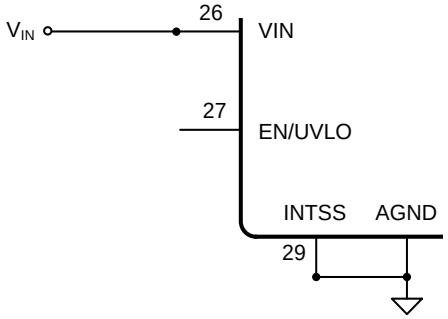

Figure 5. EN/UVLO configuration without resistive divider

Without an Enable divider (Figure 5), this MagI³C Power Module will attempt to turn on around 2.5V (V_{UVLO} voltage threshold referenced to V_{IN} pin26). This would not be useful for a stage that ultimately might be creating 5Vout. Operation of the module on input voltage conditions below the nominal output should be avoided. Systems that don't implement the Enable divider will turn in early during the rise of Vin and might not have monotonic rise in output voltage. Many systems need smooth rise in supply voltage. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the MagI³C power module output rail.

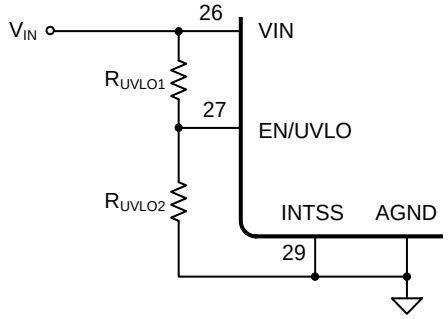

Figure 6. Undervoltage Lockout (UVLO) Schematic

Using the external enable divider R_{UVLO1} and R_{UVLO2} as shown in Figure 6, the designer is able to precisely select the turn-on and turn-off thresholds of this MagI³C Power Module. At turn-on, the V_{ON} UVLO threshold determines the input voltage level where the device begins power conversion. During the power-down sequence, the V_{OFF} UVLO threshold determines the input voltage where power conversion ceases.

The V_{ON} UVLO threshold must be set to at least (V_{OUT} + 3 V) or 6.5 V whichever is higher to insure proper startup and reduce current surges on the host input supply as the voltage rises. If possible, it is recommended to set the UVLO threshold to approximately 80% to 85% of the minimum expected input voltage.

V_{OFF} should be selected to be at least 500 mV less than V_{ON}.

Use equation 6 and 7 to calculate the values of R_{UVLO1} and R_{UVLO2}.

$$R_{UVLO1} = \frac{V_{ON} - V_{OFF}}{2.9 * 10^{-3}}\ k\Omega \qquad (10)$$

$$R_{UVLO2} = \frac{1.25}{\frac{V_{ON} - 1.25}{R_{UVLO1}} + 0.9 * 10^{-3}} k\Omega \qquad (11)$$

Table 4 lists standard resistor values for R_{UVLO1} and R_{UVLO2} for adjusting the V_{ON} UVLO threshold for several input voltages.

V_{ON} Threshold	R_{UVLO1}	R_{UVLO2}
6.5V	174kΩ	40.2kΩ
10V		24.3kΩ
15V		15.8kΩ
20V		11.5kΩ
25V		9.09kΩ
30V		7.5kΩ
35V		6.34kΩ
40V		5.62kΩ
45V		4.99kΩ

Table 4: Standard $V_{ON\ Threshold}$ Values

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Step 7 Optional: Enable / Disable

The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.
Figure 7 shows the typical application of the enable function. The EN pin has an internal pull-up current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use an open drain/collector device, or a suitable logic gate to interface with the pin.
Turning Q1 on applies a low voltage to the enable (EN) pin and disables the output of the supply shown in Figure 9. If Q1 is turned off, the supply executes a soft-start power-up sequence, as shown in Figure 8. A regulated output voltage is produced within 5ms.

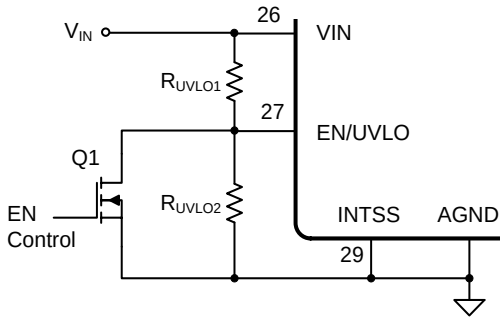


Figure 7. Typical Enable/Disable Control

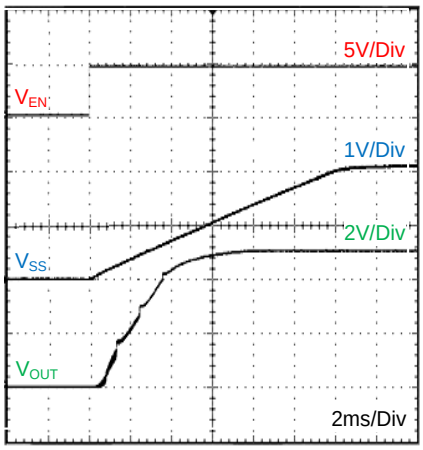


Figure 8. EN start-up I_{OUT} = 2A

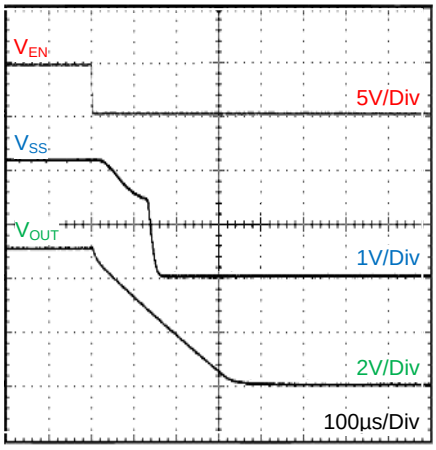


Figure 9. EN shutdown I_{OUT} = 2A

Step 8 Optional: Voltage tracking

In some applications where a digital IC with 2 or more V_{CC} pins are supplied by the power modules the simultaneous voltage rise on those pins during start up might be required (see Figure 11). Typical examples are, power supply of most FPGAs, DSPs, or other microprocessors. In these systems the higher voltage, V_{OUT1}, usually powers the I/O, and the lower voltage, V_{OUT2}, powers the core.
This can be realized using the tracking function of the MagI³C Power Module. One module (often the higher output rail) is set up as the master (see Figure 10, Module 1). The slave module (Module 2) has to be connected via the resistive divider $R1_{TR}$ and $R2_{TR}$ to the output voltage rail of the primary voltage rail (V_{OUT1}). The slave module output voltage is lower than that of the master. A typical power up sequence would start at t_0 by setting the EN pin to a level above the V_{EN} threshold to turn on Module 1. After a short delay both output voltages start rising simultaneously. The lower output voltage (V_{OUT2}) reaches it's nominal level first at time t_1. The master module reaches it's nominal level (V_{OUT1}) later at t_2. Proper configuration allows the slave rail to power up coincident with the master rail such that the voltage difference between the rails during ramp-up is small (i.e.<0.15V typ). The values for the tracking resistive divider should be selected such that the effect of the internal 2µA current source is minimized. In most cases the ratio of the tracking divider resistors is the same as the ratio of the output voltage setting divider. Proper operation in tracking mode dictates the soft-start time of the slave rail to be shorter than the master rail. Therefore place an external soft-start capacitor at the master module1.

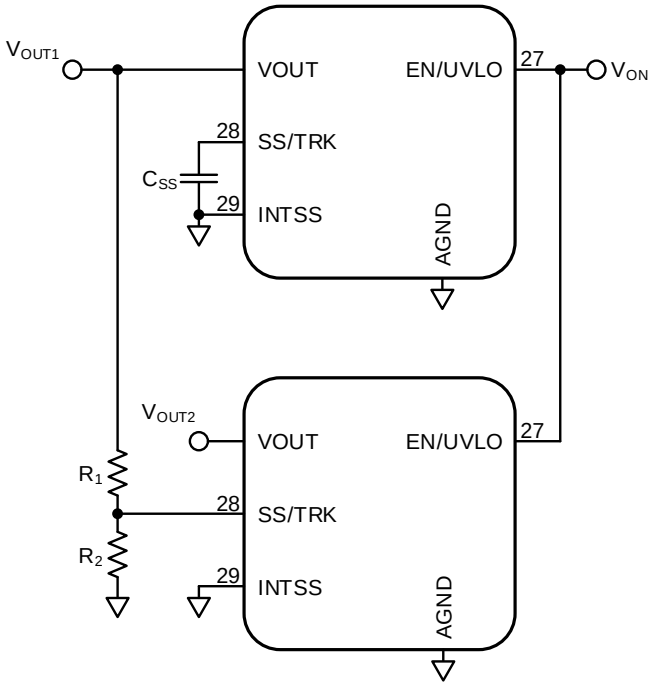


Figure 10. Voltage tracking configuration

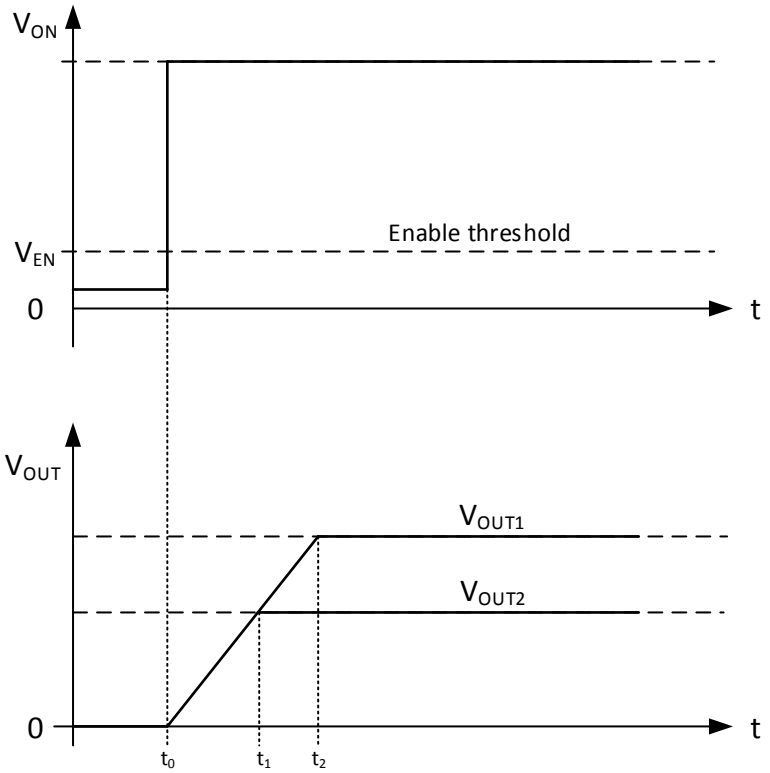


Figure 11. Simultaneous voltage tracking waveforms

First select $R2_{TR}$. A value below 10K is recommended. Use equation 8 to calculate the resistor $R1_{TR}$.

$$R1_{TR} = \left(\frac{V_{OUT2}}{0.8} - 1\right) * R2_{TR} \qquad (12)$$

For proper operation the following condition must be assured:

$$V_{OUT2} < 0.8 * V_{OUT1} \qquad (13)$$

Step 9 Optional: Synchronization to an external clock

An internal phase locked loop (PLL) allows synchronization between 300 kHz and 1 MHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle between 20 % to 80 %. The clock signal amplitude must transition lower than 0.8 V and higher than 2.0 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin. In applications where both RT mode and CLK mode are needed, the device can be configured as shown in Figure 12.
Before the external clock is present, the device works in RT mode where the switching frequency is set by the R_{RT} resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the CLK pin is pulled above the RT/CLK high threshold (2.0 V), the device switches from RT mode to CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from CLK mode back to RT mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by the R_{RT} resistor.

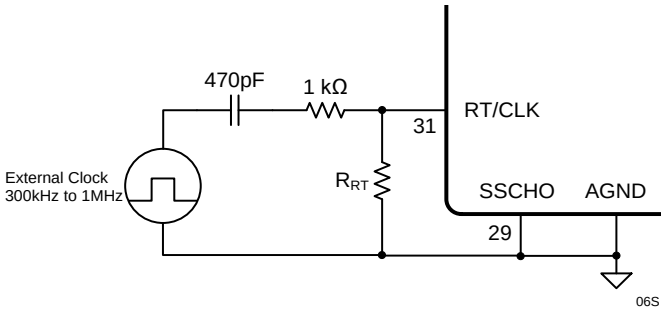
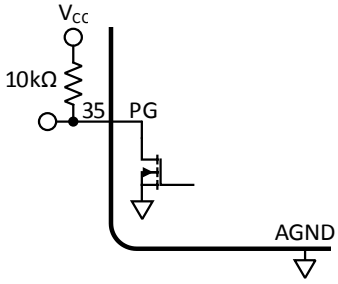


Figure 12. Synchronization Configuration

Step 10 Optional: Power Good (PG)

The PG pin is an open drain output. Once the output voltage is between 94 % and 106 % of the set voltage, the PG pin pull-down is released and the pin floats. The recommended pull-up resistor value is between 10 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. The PG pin is in a defined state once V_{IN} is higher than 1.0 V, but with reduced current sinking capability. The PG pin achieves full current sinking capability once the V_{IN} pin is above 4.5 V. The PG pin is pulled low when the output voltage is lower than 91 % or higher than 109 % of the nominal set voltage. Also, the PG pin is pulled low if the input UVLO or thermal shutdown is asserted, the EN pin is pulled low, or the SS/TRK pin is below 1.4 V.



V_{CC} = V_{IN} or other supply voltage below 5.5V

Light Load Operation

The MagI³C Power Module is a non-synchronous converter. One of its characteristics is, that as the load current on the output is decreased a point is reached where the energy delivered by a single switching pulse is more than the load can absorb. This causes the output voltage to rise slightly. This rise in output voltage is sensed by the feedback loop and the device responds by skipping one or more switching cycles until the output voltages falls back to the set point. At very light loads or no load, many switching cycles are skipped. The observed effect during this pulse skipping mode of operation is an increase in the peak to peak ripple voltage, and a decrease in the ripple frequency. The load current at which pulse skipping begins is a function of the input voltage, the output voltage, and the switching frequency. A plot of the pulse skipping threshold current as a function of input voltage is given in Figure 13 for a number of popular output voltage and switching frequency combinations.

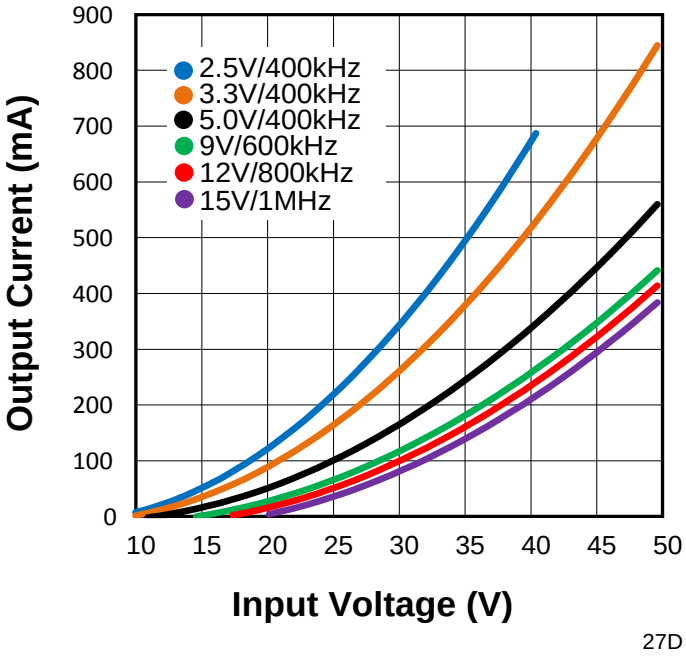


Figure 13. Pulse Skipping Load Threshold

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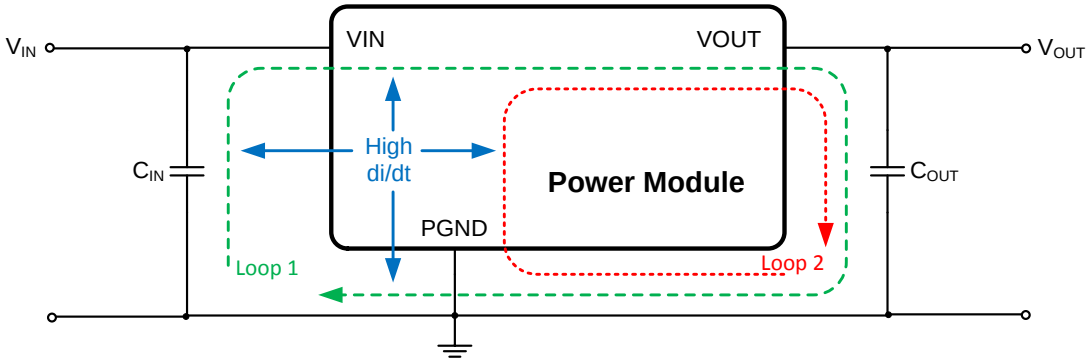
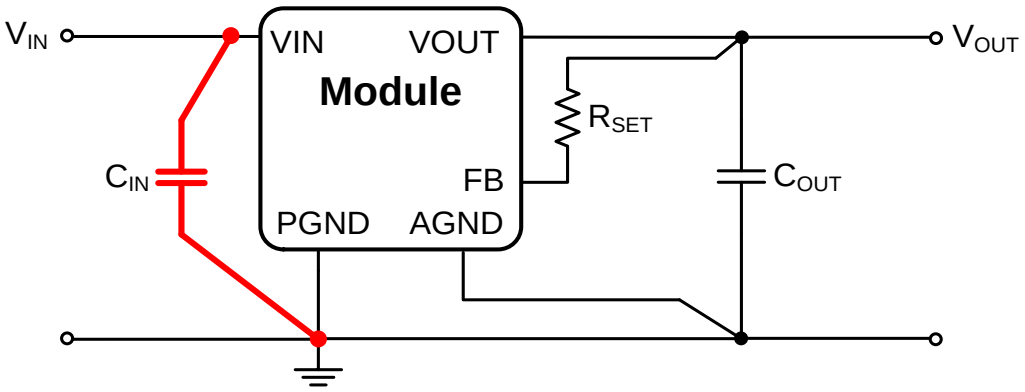
PCB Layout Instructions:

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following five simple design rules.

1: Minimize area of switched current loops



Target is to identify the paths in the system which have discontinuous current flow. They are the most critical ones because they act as an antenna and cause observable high frequency noise (EMI). The easiest approach to find the critical paths is to draw the high current loops during both switching cycles and identify the sections which do not overlap. They are the ones where no continuous current flows and high di/dt is observed. Loop 1 is the current path during the ON-time of the High-Side MOSFET. Loop 2 is the current path during the OFF-time of the High-Side MOSFET.



Based on those considerations, the path of the input capacitor C_{IN} is the most critical one to generate high frequency noise on Vin. Therefore place C_{IN} as close as possible to the MagI³C power module V_{IN} and PGND pins. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the PGND pins.

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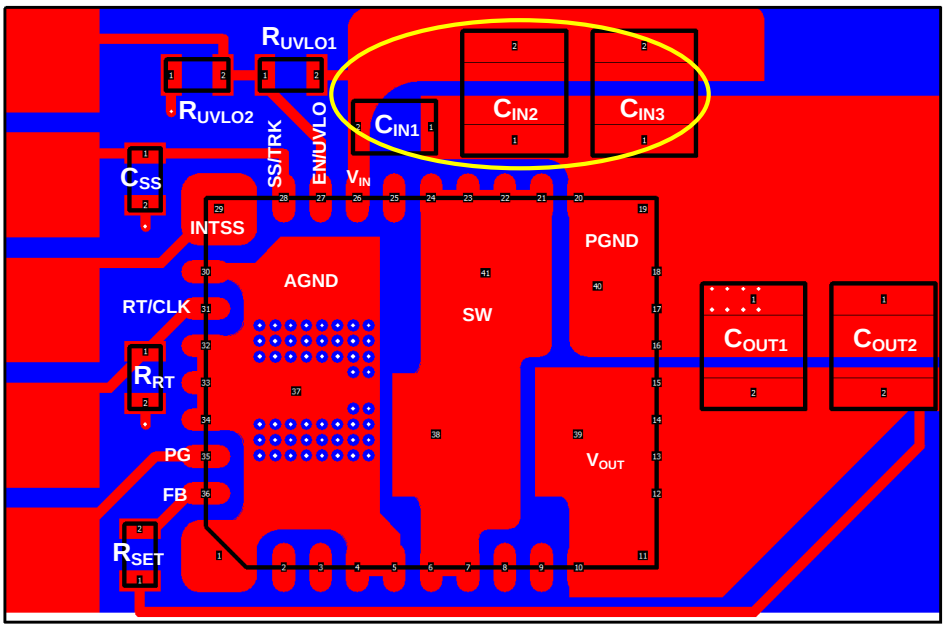
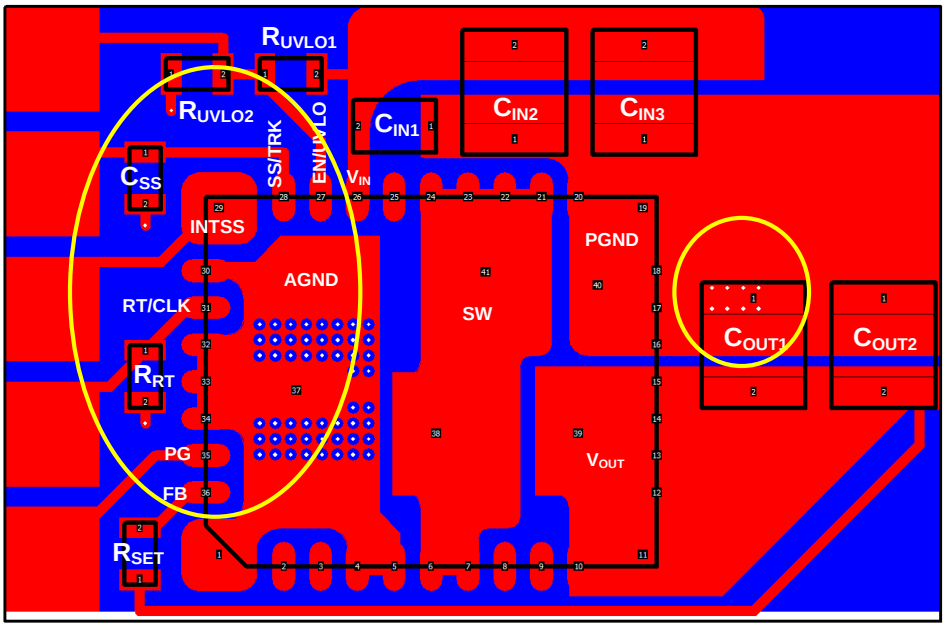
The placement of the input capacitors is highlighted in the following picture of the reference board:



2: Have a single point ground
The ground connections for the clock setting, soft-start, and enable components should be routed to the AGND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior.

Connect the AGND and PGND copper area at one point at the ground terminal of the first output capacitor.



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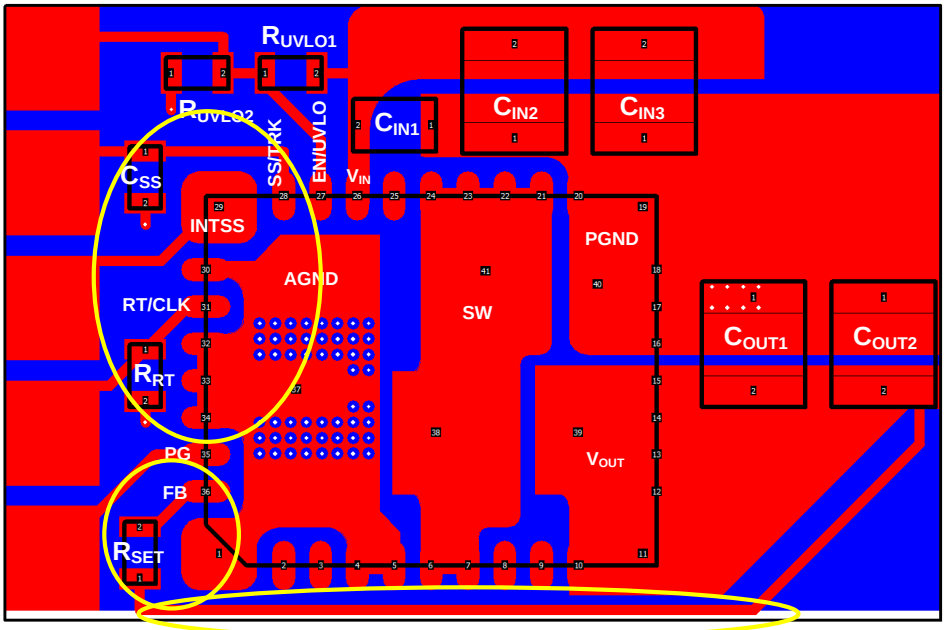
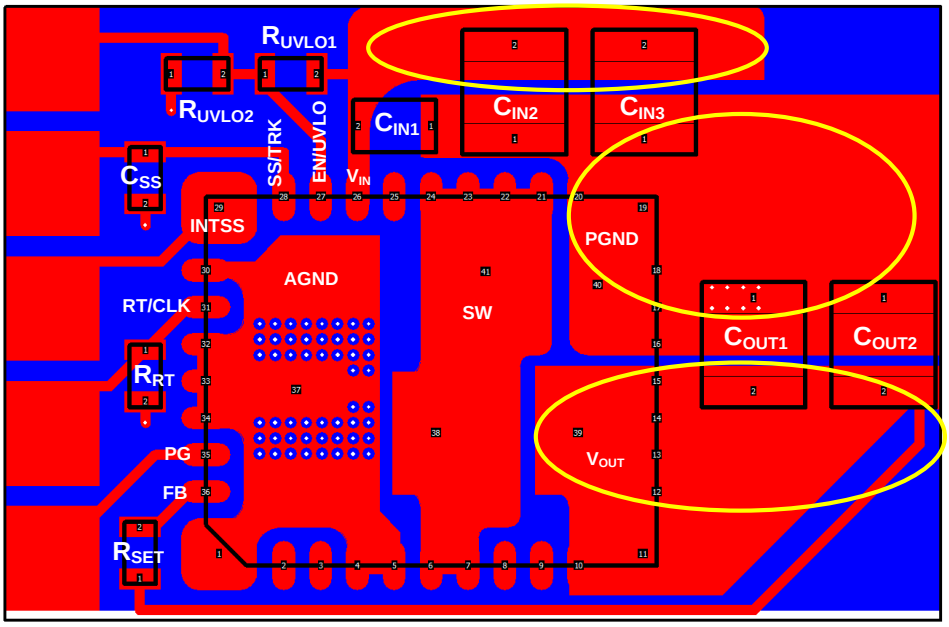
3: Minimize trace length to high impedance pins
The feedback resistor, R_{SET} should be located close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The traces from R_{SET} should be routed away from the body of the MagI³C power module to minimize noise pickup.

Place R_{RT}, and C_{SS} as close as possible to their respective pins.



4: Make input and output terminal connections as wide as possible
This reduces any voltage drops on the input or output of the converter and maximizes efficiency.



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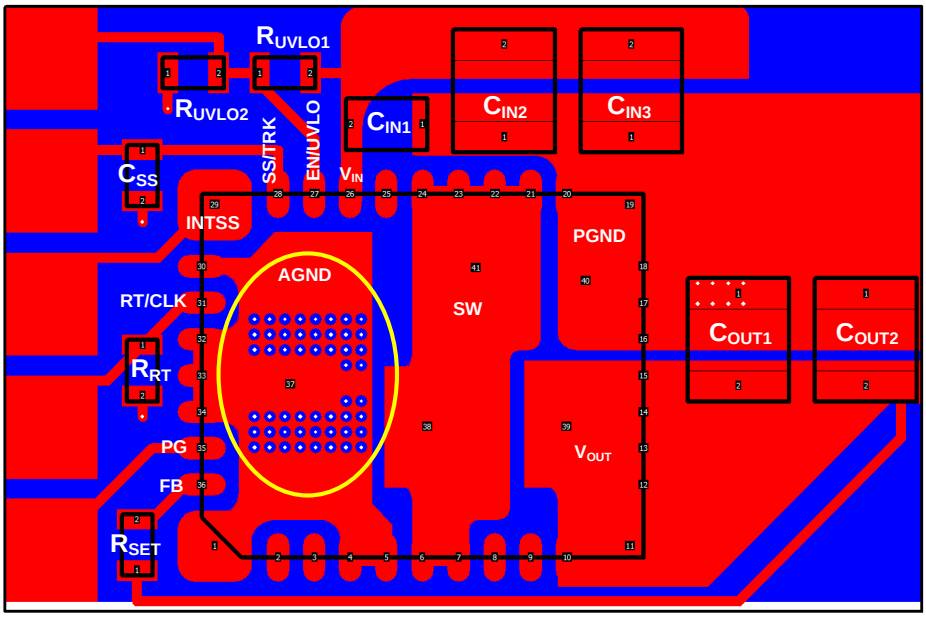
5: Provide adequate device heat-sinking

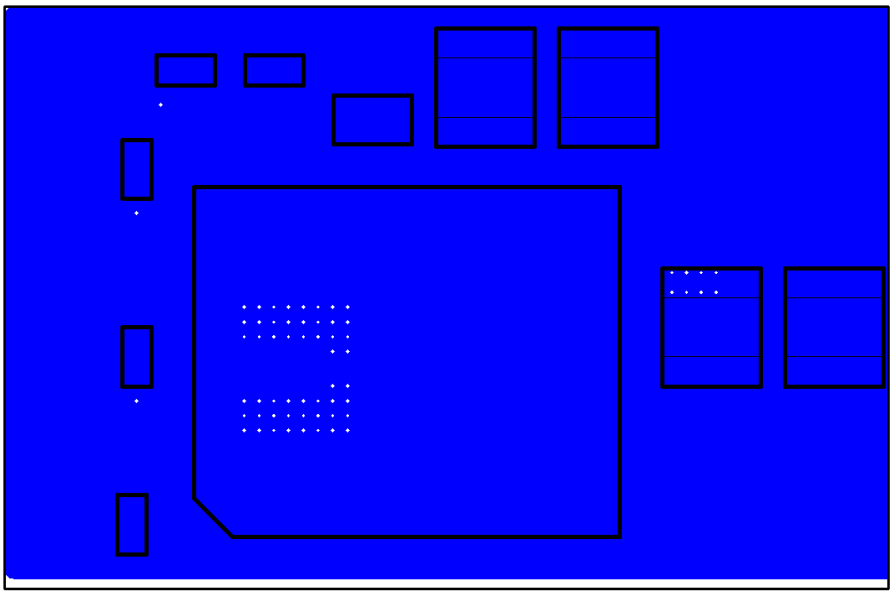
Place a dedicated AGND copper area beneath the MagI³C Power Module.



Use an array of heat-sinking vias to connect the AGND pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be used to make connection to inner layer heat-spreading ground planes. It is recommended to use a via array as proposed in the picture above with via diameter of 300µm (hole:100µm) thermal vias spaced 400µm. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

6: Isolate high noise areas

Place a dedicated AGND copper area beneath the MagI³C Power Module.



Determine power losses and thermal requirements of the board

For example:

$V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 1.5A, T_{AMB(MAX)} = 85°C$ and $T_{J(MAX)} = 125°C$

$T_{AMB(MAX)}$ is the maximum air temperature surrounding the module.
$T_{J(MAX)}$ is the maximum value of the junction temperature according to the "OPERATING CONDITIONS" limit.

The goal of the calculation is to determine the characteristics of the required heat sink. In case of a surface mounted module this would be the PCB (number of layers, copper area and thickness). These characteristics are reflected in the value of the thermal resistance case to ambient: θ_{CA}.

The basic formula for calculating the operating junction temperature T_J of a semiconductor device is as follows:

$$T_J = P_{IC-Loss} * \theta_{JA} + T_{AMB} \qquad (14)$$

$P_{IC-LOSS}$ are the total power losses within the module IC and are related to the operating conditions.
θ_{JA} is the thermal resistance junction to ambient and calculated as:

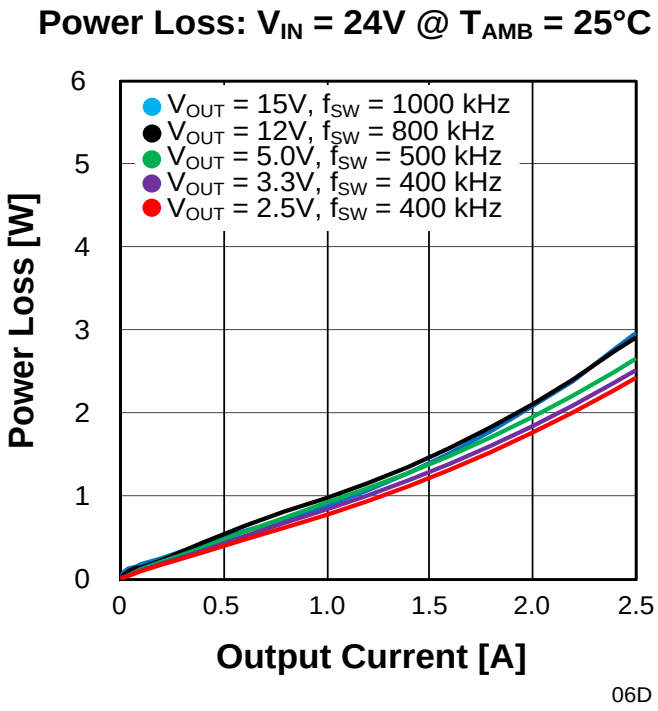
$$\theta_{JA} = \theta_{JC} + \theta_{CA} \qquad (15)$$

θ_{JC} is the thermal resistance junction to case.

Combining equation (14) and (15) results in the maximum case-to-ambient thermal resistance:

$$\theta_{CA(MAX)} < \frac{T_{J-MAX} - T_{AMB(MAX)}}{P_{IC-Loss}} - \theta_{JC} \qquad (16)$$

From section "THERMAL SPECIFICATIONS" use as typical thermal resistance from junction to case $\theta_{JC} = \theta_{JB} = 6.8$ °C/W. Use the 25°C power dissipation curves in the "TYPICAL PERFORMANCE CURVES" section to estimate the $P_{IC-LOSS}$ for the application being designed. Add 20% losses to take into consideration the ambient temperature of 85°C.



From the graph we read a power loss of 1.5W. Adding 20% results in a loss of 1.8W. Entering the values in formula (16) results in:

$$\theta_{CA(MAX)} < \frac{125°C - 85°C}{1.8W} - 6.8°C/W = 15.42°C/W$$

$$\theta_{JA(MAX)} = \theta_{JC} + \theta_{CA(MAX)} = 6.8°C/W + 15.42°C/W = 22.2°C/W$$

To achieve this thermal resistance the PCB is required to dissipate the heat effectively. The area of the PCB will have a direct effect on the overall junction-to-ambient thermal resistance.

For $\theta_{JA} < 22.2°C/W$ and only natural convection (i.e. no air flow), the minimum PCB area should be slightly smaller than 60cm^2. This corresponds to a square board with 7,6 cm x 7,6 cm copper area, 4 layers, and 35µm copper thickness. Higher copper thickness will further improve the overall thermal performance. Note that thermal vias should be placed under the IC package to easily transfer heat from the top layer of the PCB to the inner layers and the bottom layer.

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PROTECTIVE FEATURES

Over current protection (OCP)

For protection against load faults, the MagI³C Power Module incorporates cycle-by-cycle current limiting. During an overcurrent condition the output current is limited and the output voltage is reduced, as shown in Figure 14. As the output voltage drops more than 8% below the set point, the PG signal is pulled low. If the output voltage drops more than 25% during an overcurrent condition, the module skips switching cycles to reduce power dissipation within the device. When the overcurrent condition is removed, the output voltage returns to the established voltage. The MagI³C Power Module is not designed to endure a sustained short circuit condition. The use of an output fuse, voltage supervisor circuit, or other overcurrent protection circuit is recommended. A recommended overcurrent protection circuit is shown in Figure 15. This circuit uses the PG signal as an indication of an overcurrent condition. As PG remains low, the TLC555 timer operates as a low frequency oscillator, driving the EN/UVLO pin low for approximately 400ms, halting the power conversion of the device. After the inhibit interval, the EN/UVLO pin is released and the MagI³C Power Module restarts. If the overcurrent condition is removed, the PG signal goes high, resetting the oscillator and power conversion resumes, otherwise the inhibit cycle repeats.

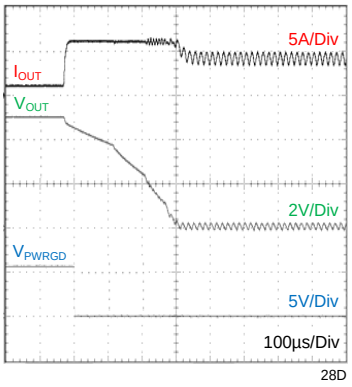

Figure 14. Overcurrent Limiting

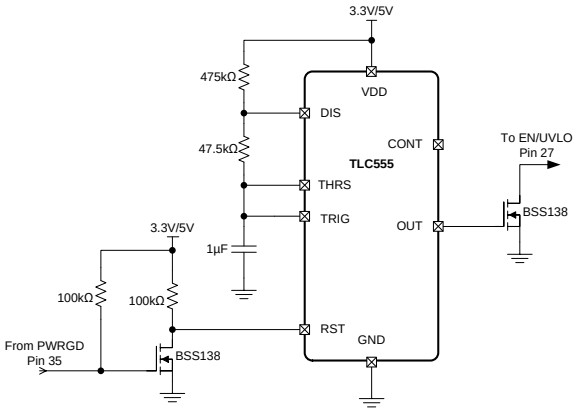

Figure 15. Over-Current Protection Circuit

Over temperature protection (OTP)

The junction temperature of the MagI³C power module should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal thermal shutdown circuit which activates at 180°C (typ) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_{OUT} to fall, and additionally the C_{SS} capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 165° the SS pin is released, V_{OUT} rises smoothly, and functional operation resumes. Please note that an operation of the junction above 125°C is not recommended.
Applications requiring maximum output current especially those at high input voltage may require additional derating at elevated temperatures

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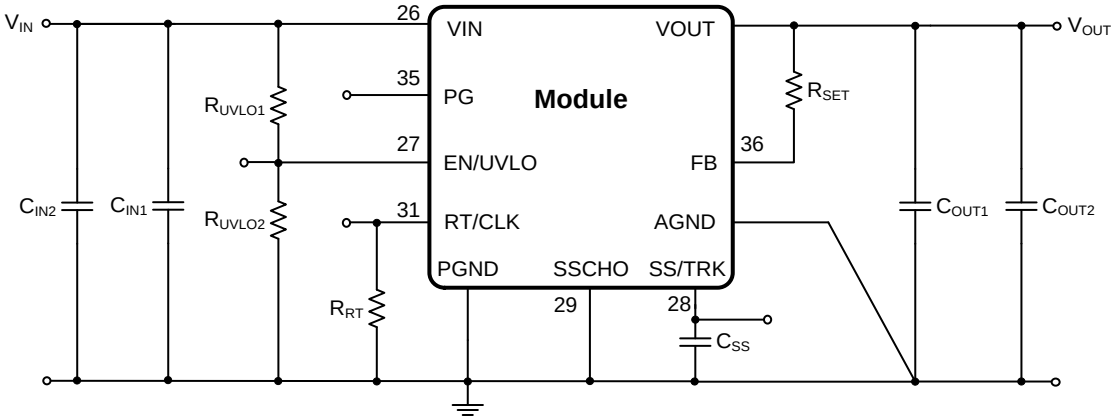
APPLICATIONS

Typical Application Circuit



Recommended component values specified at T_A = 25°C

V_{OUT}	12V	5V	3.3V
V_{IN}	15V to 50V	8V to 50V	7V to 36V
R_{SET}	140kΩ	52.3kΩ	31.6kΩ
R_{UVLO1}	174kΩ	174kΩ	174kΩ
R_{UVLO2}	15.4kΩ	31.6kΩ	40.2kΩ
R_{RT}	267kΩ	1.1MΩ	Open
$C_{IN1\ min}$	2.2µF; 100V	2.2µF; 100V	4.7µF; 50V
C_{IN2}	2.2µF; 100V	2.2µF; 100V	Open
$C_{OUT1\ min}$	47µF; 16V	47µF; 6.3V	47µF; 6.3V
C_{OUT2}	47µF; 16V	47µF; 6.3V	47µF; 6.3V
C_{SS}	22nF	Open	Open

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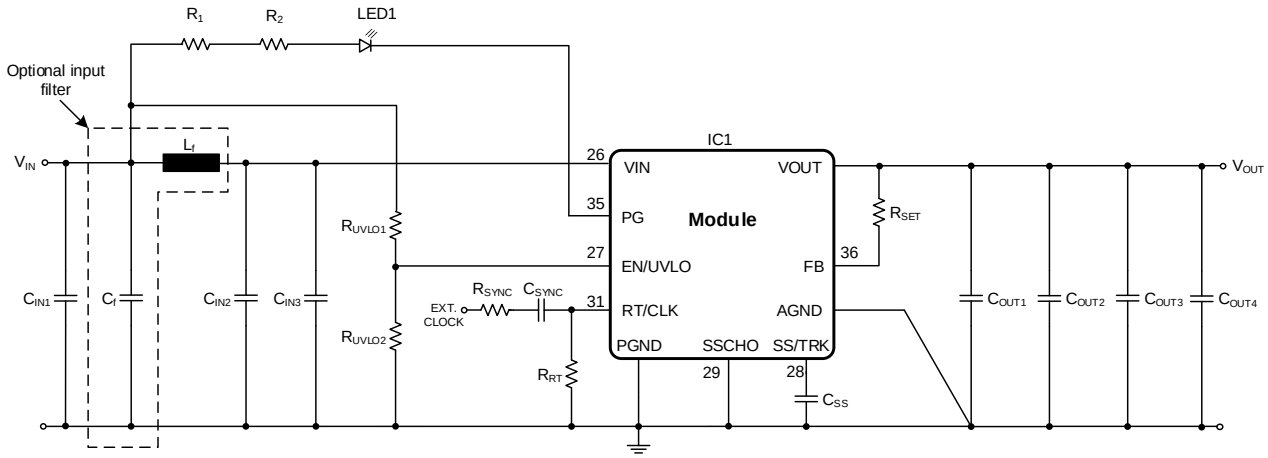
EVALUATION BOARD SCHEMATIC



Bill of Material

Designator	Description		Quantity	Order Code	Manufacturer
IC1	MagI³C Power Module		1	171021501	Würth Elektronik
C_{IN1}	Aluminium Electrolythic capacitor 27µF/100V		1	860040874001	Würth Elektronik
C_{IN2},C_{IN3}	Ceramic chip capacitor 4,7µF/100V X5R		2		
C_{OUT1}	Ceramic chip capacitor 100nF/100V X7R 0805		1		
C_{OUT2},C_{OUT3}	Ceramic chip capacitor 22µF/25V X7R		2	885012109014	Würth Elektronik
C_{OUT4}	Aluminium Polymer Electrolythic capacitor 33µF/25V		1	875105545004	Würth Elektronik
C_{SS}, C_{SYNC}	Not mounted				
C_f (1)	Filter ceramic chip capacitor 2.2µF/100V		1		
L_f (2)	Filter inductor 22µH, PD2		1	744774122	Würth Elektronik
R_{UVLO1},R_{UVLO2}, R_{SYNC}	Not mounted				
R_1	12.4kΩ		1		
R_2	12.4kΩ		1		
LED1	LED red		1	150080SS75000	Würth Elektronik
R_{RT}	Set by jumper	Open for f_{sw} = 400kHz			
		1.1MΩ for f_{sw} = 500kHz	1		
		549kΩ for f_{sw} = 600kHz	1		
		365kΩ for f_{sw} = 700kHz	1		
		267kΩ for f_{sw} = 800kHz	1		
		215kΩ for f_{sw} = 900kHz	1		
		178kΩ for f_{sw} = 1MHz	1		
R_{SET}	Set by jumper	21.5kΩ for V_{OUT} = 2.5V	1		
		31.6kΩ for V_{OUT} = 3.3V	1		
		52.3kΩ for V_{OUT} = 5V	1		
		102kΩ for V_{OUT} = 9V	1		
		140kΩ for V_{OUT} = 12V	1		
		178kΩ for V_{OUT} = 15V	1		

(1) not mounted on the Evaluation Board
(2) not mounted on the Evaluation Board. A shorting wire or 0R resistor is put in its place

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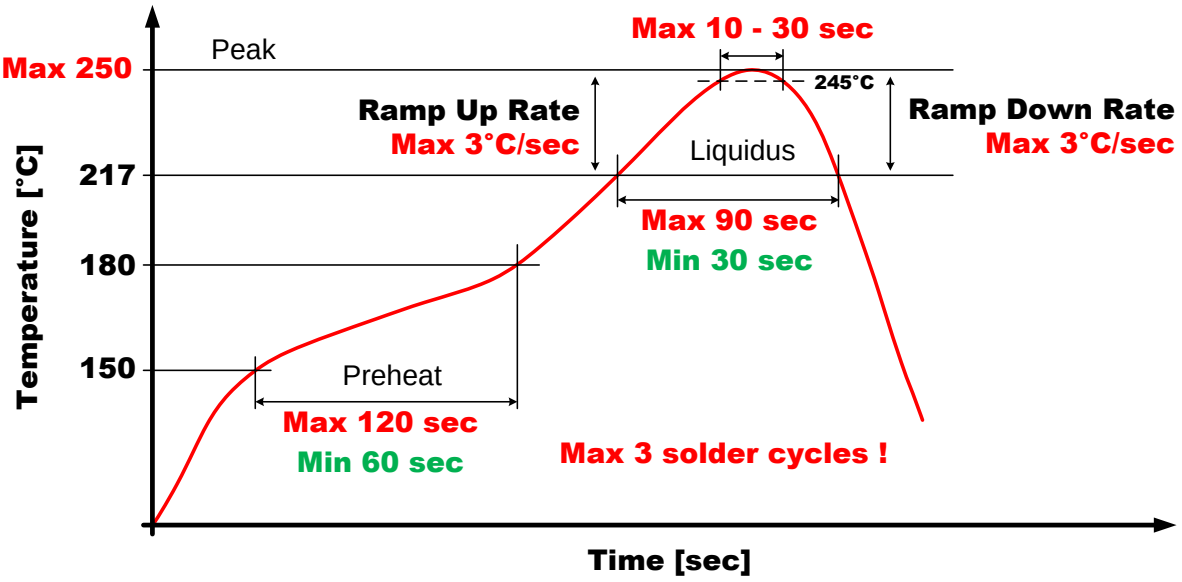
HANDLING RECOMMENDATIONS

1. f

SOLDER PROFILE

1. Only Pb-Free assembly is recommended according to JEDEC J-STD020.
2. Measure the peak reflow temperature of the MagI³C power module in the middle of the top view.
3. Ensure that the peak reflow temperature does not exceed 245°C ±5°C as per JEDEC J-STD020.
4. The reflow time period during peak temperature of 245°C ±5°C must not exceed 30 seconds.
5. Reflow time above liquidus (217°C) must not exceed 90 seconds.
6. Maximum ramp up is rate 3°C per second
7. Maximum ramp down rate is 3°C per second
8. Reflow time from room (25°C) to peak must not exceed 8 minutes as per JEDEC J-STD020.
9. **Maximum numbers of reflow cycles is three**.
10. **For minimum risk, solder the module in the last reflow cycle of the PCB production.**
11. For soldering process please consider lead material copper (Cu) and lead finish tin (Sn).
12. For solder paste use a standard SAC Alloy such as SAC 305, type 3 or higher.
13. Below profile is valid for convection reflow only
14. Other soldering methods (e.g.vapor phase) are not verified and have to be validated by the customer on his own risk



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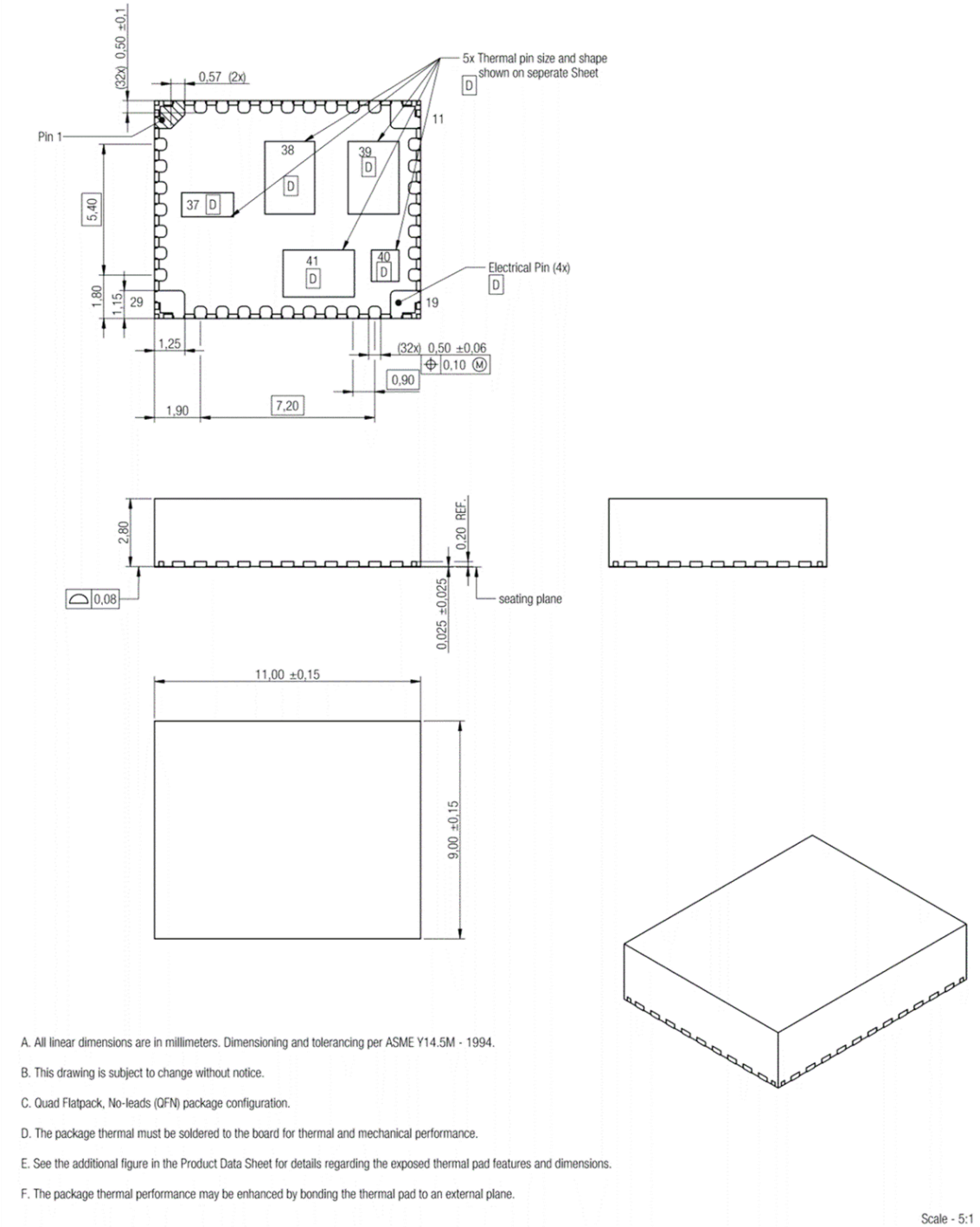
PHYSICAL DIMENSIONS (mm)

Package Type: BQFN-41 (9 x 11 x 2.8mm)



A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M - 1994.

B. This drawing is subject to change without notice.

C. Quad Flatpack, No-leads (QFN) package configuration.

D. The package thermal must be soldered to the board for thermal and mechanical performance.

E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

F. The package thermal performance may be enhanced by bonding the thermal pad to an external plane.

Scale - 5:1

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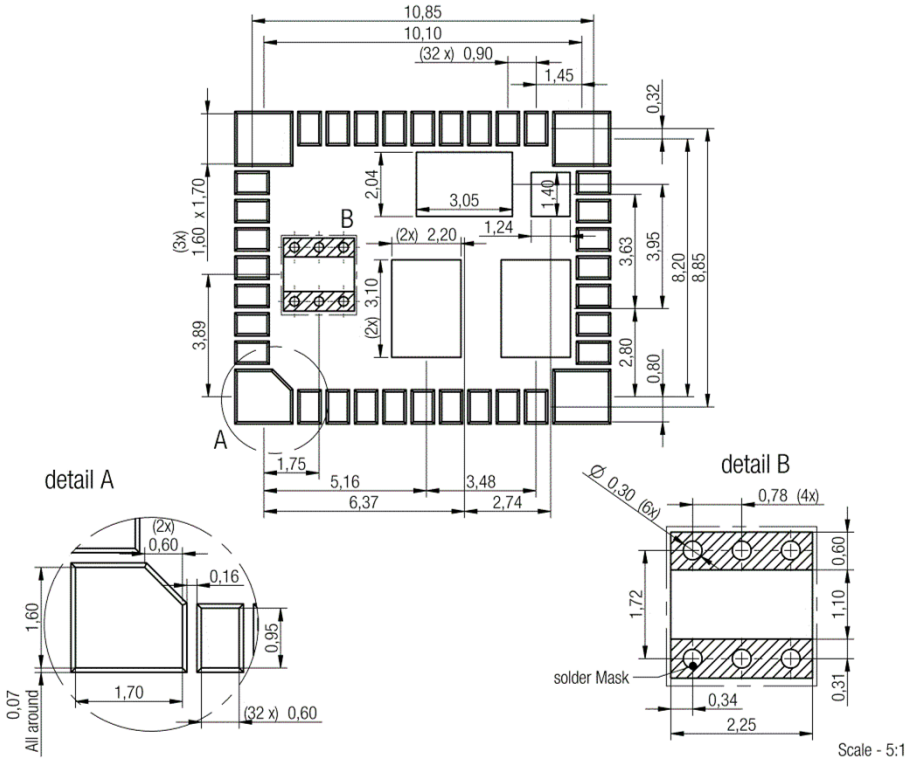

recommended soldering pad
solder past recommendation 150 µm

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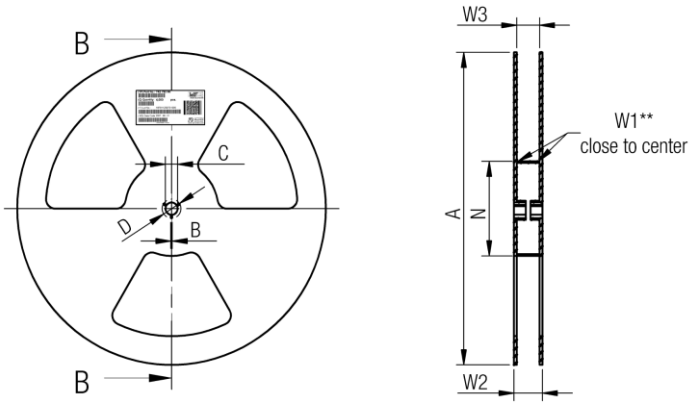
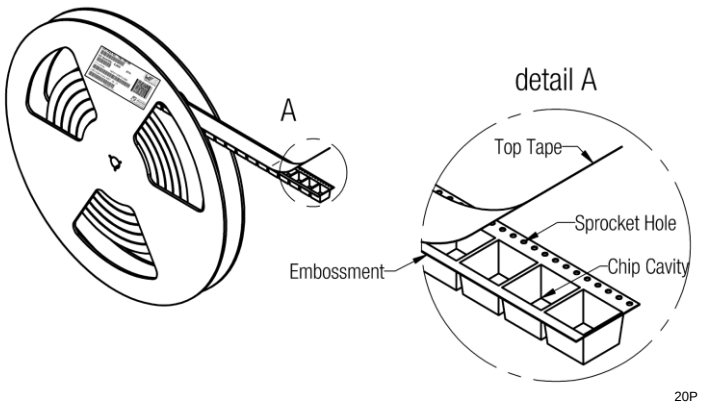
PACKAGING

Reel (mm)



		A	B	C	D	N	W1	W2	W3	W3
tolerance		± 2,0	min.	± 0,8	min.	± 2,0	+ 2	max.	min.	max.
Tape width	**24mm**	330,00	1,50	13,00	20,20	60,00	24,40	30,40	23,90	27,40



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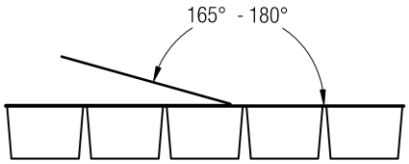
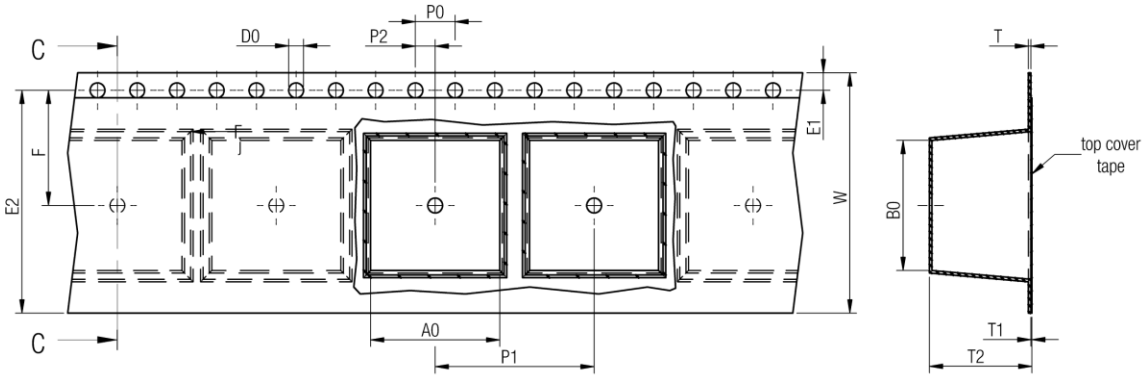
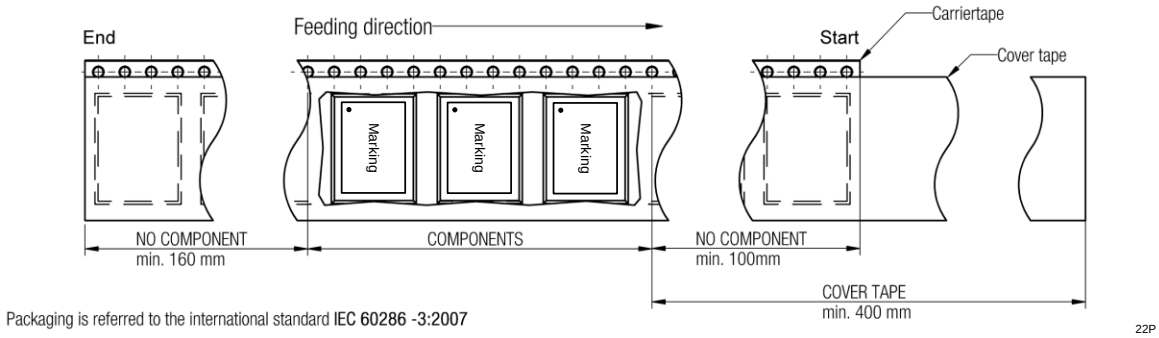
Tape (mm)



		Pull-of force
Tape width	**24 mm**	0,1 N - 1,3 N



		A0	B0	W	P1	T	T1	T2	D0	E1	E2	F	P0	P2	Tape	VPE / packaging unit
tolerance		±0,1	±0,1	+0,3 -0,1	± 0,1	±0,05	max.	±0,1	±0,05	± 0,1	min.	± 0,05	± 0,1	±0,10		
size	**BQFN-41**	9,35	11,35	24,00	16,00	0,30	0,10	3,10	1,55	1,75	22,25	11,50	4,00	2,00	Polystyrene	250



Packaging is referred to the international standard IEC 60286 -3:2007

22P

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DOCUMENT HISTORY

Revision	Date	Description	Comment
1.0	May 2016	Release of final version	

CAUTIONS AND WARNINGS

The following conditions apply to all goods within the product series of MagI³C of Würth Elektronik eiSos GmbH & Co. KG:

General:
All recommendations according to the general technical specifications of the data-sheet have to be complied with.

The usage and operation of the product within ambient conditions which probably alloy or harm the component surface has to be avoided.

The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products.

Residual washing varnish agent that is used during the production to clean the application might change the characteristics of the body, pins or termination. The washing varnish agent could have a negative effect on the long term function of the product.
Direct mechanical impact to the product shall be prevented as the material of the body, pins or termination could flake or in the worst case it could break. As these devices are sensitive to electrostatic discharge customer shall follow proper IC Handling Procedures.

Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KG components in its applications, notwithstanding any applications-related information or support that may be provided by Würth Elektronik eiSos GmbH & Co. KG. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Customer will fully indemnify Würth Elektronik eiSos and its representatives against any damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications.

Product specific:
Follow all instructions mentioned in the datasheet, especially:
- The solder profile has to comply with the technical reflow or wave soldering specification, otherwise this will void the warranty.
- All products are supposed to be used before the end of the period of 12 months based on the product date-code.
- Violation of the technical product specifications such as exceeding the absolute maximum ratings will void the warranty.
- It is also recommended to return the body to the original moisture proof bag and reseal the moisture proof bag again.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

WPMDU1251501 / 171021501

MagI³C Power Module
VDRM - Variable Step Down Regulator Module

IMPORTANT NOTES

The following conditions apply to all goods within the product range of Würth Elektronik eiSos GmbH & Co. KG:

1. General Customer Responsibility
Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that the datasheet is current before placing orders.

2. Customer Responsibility related to Specific, in particular Safety-Relevant Applications
It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

3. Best Care and Attention
Any product-specific notes, warnings and cautions must be strictly observed.

4. Customer Support for Product Specifications
Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

5. Product R&D
Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard we inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

6. Product Life Cycle
Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC-Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

7. Property Rights
All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG. Würth Elektronik eiSos GmbH & Co. KG does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, application, or process in which Würth Elektronik eiSos GmbH & Co. KG components or services are used.

8. General Terms and Conditions
Unless otherwise agreed in individual contracts, all orders are subject to the current version of the “General Terms and Conditions of Würth Elektronik eiSos Group”, last version available at www.we-online.com.