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QorIQ Qonverge

QorIQ Qonverge Platform

QorIQ Qonverge B4420 Baseband Processor

A smarter approach to metrocell baseband processing

Overview

QorIQ Qonverge B4420 multicore system-on-chip (SoC) architecture is designed for high-performance wireless infrastructure applications. It provides ultra-high performance for small cell base station platforms supporting various wireless standards including WCDMA (HSPA/HSPA+), FDD-LTE, TDD-LTE and LTE-Advanced including 3GPP LTE Rel.10/11.

Macrocell base-station-only networks cannot support the increasing demand for bandwidth as throughputs degrade significantly over distance and in highly populated metropolitan areas, resulting in the need to bring the base station closer to the end user. Solving the mobile broadband challenges of delivering WCDMA (HSPA+), LTE and LTE-Advanced to a high number of users and managing an increase in data throughputs in a cost-effective manner is essential to augment a large number of metrocell base stations to the macrocell network. To effectively deploy these small base stations, operators and OEMs need to deliver high throughput and high user capacity at low power and cost.

Addressing these requirements is the QorIQ Qonverge B4420 device, a multi-standard wireless base station SoC based on 28 nm advanced process technology, delivering capacity of up to dual-sector LTE or quad-carrier HSPA and supporting multi-mode operation for several hundred simultaneous users, high downlink and uplink data throughputs with optimal cost and power.

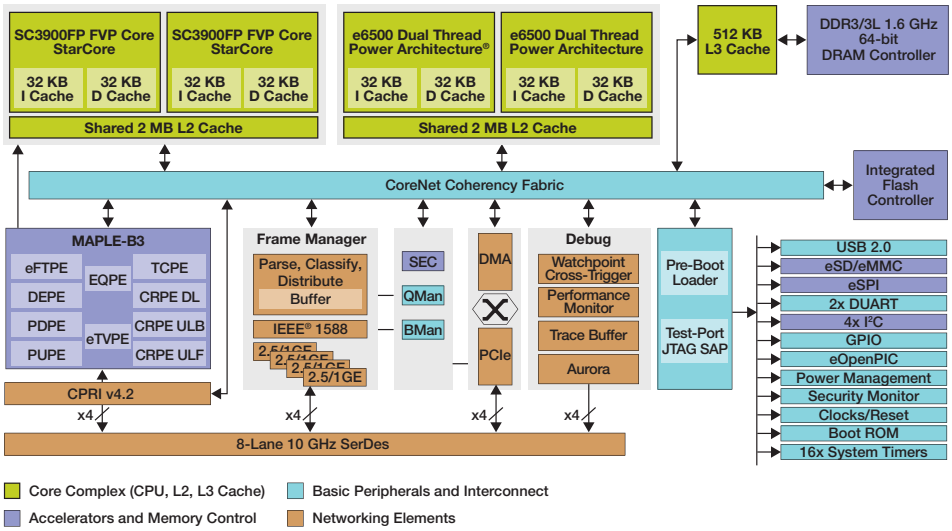
This multicore SoC includes four programmable cores, two 64-bit Power Architecture® cores and two cores based on a StarCore flexible vector processor (FVP) and high throughput, low latency hardware accelerators to enable highly optimized processing for the radio processing chain, from PHY to transport layers.

The B4420 baseband processor is a highly programmable solution that targets wireless operators' infrastructure deployments and builds upon our proven success of the existing multicore SoCs, MPUs and DSPs in wireless infrastructure markets. It delivers the complete digital processing chain, from antenna IQ samples to backhaul IP networks.

QorIQ Qonverge B4420 provides a programmable platform where layer 2 scheduling, control and transport processing are implemented using a mix of e6500 Power Architecture 64-bit dual threaded cores, SIMD engines, data path and security accelerators. Layer 1 radio processing is implemented using a mix of StarCore SC3900FP high-performance FVP cores and the flexible Multi-Accelerator Platform Engine for Baseband (MAPLE-B), which provides a highly efficient hardware implementation for FEC decoding and encoding, Fast Fourier transforms, embedded PDSCH and PUSCH processing chains, MiMO equalization and WCDMA chip rate.

The smart partitioning introduced in the QorIQ Qonverge platform provides an excellent balance for programming of the different radio processing layers, enabling OEMs, Freescale and its partners to leverage software and intellectual property using the fully programmable cores along with hardwired accelerators and high internal bandwidth for non-blocking accesses to all processing cores, coprocessors and peripherals to deliver a highly efficient solution in terms of throughputs, cost and energy efficiency.

QorIQ Qonverge B4420 Block Diagram



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In addition to the proven, field-deployed and high-performance internal fabric and baseband accelerators, the major contributions to the B4420 processor's high performance are the e6500 MPU core, which has achieved the highest CoreMark® benchmark performance-per-watt profile ever recorded for an embedded processor, and the all-new SC3900FP StarCore FVP core, which earned the highest fixed-point benchmark score ever recorded by independent signal-processing technology analysis firm Berkeley Design Technology, Inc.

Freescale scalable multicore SoC architecture solutions provide developers with a range of software-compatible devices to minimize development time and maximize reuse across all base station platforms from femto to macro. The B4420 metrocell SoC is pin and code compatible with the B4860 macrocell SoC, enabling OEMs to migrate from macro to metro/microcells reusing the same hardware design and a scaled down version of the software, allowing very fast design and product introduction.augue et adipiscing malesuada, arcu diam ultrices lectus, a ullamcorper metus massafau wisi. Morbi pellentesque nisl. Fusce dignissim fringilla risus.

QorIQ Qonverge B4420 Processor Features

Hardware

- Integrated processor cores and accelerators for layer 2, control and transport processing
  - Two e6500 dual-threaded, 64-bit Power Architecture cores up to 1.6 GHz
    - Dual threading with simultaneous multi-threading (SMT)
    - 40-bit physical addressing
    - Fully featured MMU with a 1024-entry eight-way set-associative cache
    - Core virtualization supporting hypervisor and logical to real address translation
    - 128-bit AltiVec SIMD engine
    - 2 MB clustered L2 cache allowing strict allocation or full sharing
    - Hardware support for L1 and L2 cache coherency
- Integrated DSP cores and baseband accelerators for layer 1 processing
  - Two StarCore SC3900FP FVP programmable cores up to 1.2 GHz
    - Up to 32 MAC/cycle of 16-bit and up to 16 FLOP/cycle
    - Eight instructions per cycle
    - Up to eight data lanes vector in a single instruction (SIMD8)
    - State-of-the-art support for control code with branch prediction
    - Fully featured memory management unit and logical to real address translation
    - 2 MB clustered L2 cache allowing strict allocation or full sharing
    - Hardware support for L1 and L2 cache coherency
- MAPLE baseband accelerators
  - FEC accelerators for WCDMA (HSPA/HSPA+), LTE and LTE-Advanced
    - Turbo decoder with rate de-matching and HARQ combining
    - Turbo encoder with rate matching
    - Viterbi decoder
  - FFT/iFFT, DFT/iDFT
  - MiMO equalizer MMSE-based supporting IRC, SIC and PIC
  - Matrix inversion and multiplication
  - PUSCH data path embedded processing chain
  - PDSCH data path embedded processing chain
  - WCDMA/HSPA chip rate and path search
  - CRC insertion and check
- Data Path Acceleration Architecture, including:
  - Frame manager supporting in-line packet parsing and general classification to enable policing and QoS-based packet distribution
  - Queue and buffer manager which allow offloading of queue management, task management, load distribution, flow ordering, buffer management and allocation tasks from the cores
  - Security protocols accelerators for backhaul and over-the-air including SNOW-3G,Kasumi, ZUC, IPsec, DES, 3DES, AES, MD5, SHA-1/2, HMAC
- CoreNet: Internal non-blocking switch fabric for full cache coherent system
- DDR-3/3L controller: 64-bit, 1.6 GHz with 512 KB L3 cache
- ECC support for on-chip and off-chip memories
- High-speed interfaces multiplexed into Eight SerDes lanes:
- Four 1/2.5 Gb Ethernet interfaces with IEEE® 1588v2 support
- Four CPRI v4.2 controllers 9.8G
- Four-lane PCI Express® 5G (Gen II)
- Two Aurora: Tracing/debug
- Trust architecture with secured boot
- One serial port interface (eSPI)
- One eSD/eMMC interface
- One IFC: 16-bit integrated NAND/NOR flash controller or general-purpose memory interface
- USB 2.0 interface
- Four I²C Interfaces
- Four UART ports

Software

- A complete set of development tools that includes:
  - CodeWarrior Eclipse IDE
  - Compilers and debuggers
  - Profiling, critical code analysis, call tree, trace points
  - Nexus trace viewer, code viewer, performance, view, trace analyzer
  - Scripting for post-process trace and performance data
  - Register analyzer
  - Device and core simulators
  - Operating systems
  - BSP and device drivers
- B4420QDS board: Software and reference application development system
- Freescale layer 1 reference software libraries for LTE and WCDMA (HSPA/HSPA+)
- VortiQa transport software, layer 2 software from Freescale partners

General

- 1020-pin FC-PBGA package, 1 mm ball pitch
- Core voltage: VID
- I/O voltage: 1, 1.2, 1.35, 1.5, 1.8 and 2.5 V
- Junction temperatures support commercial 0 °C to +105 °C and extended –40 °C to +105 °C
- Debug ports: Test access port and boundary scan architecture compliant with IEEE Std. 1149.1™, 1149.6™ and Nexus IEEE-ISTO 5001 trace support
- Lead-free ROHS compliant

For more information, visit freescale.com/QorIQQonverge

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